

# SEMICONDUCTOR



## Radar Scope

LTX announced that **Accelerix** has purchased and taken delivery of a Delta STE, configurable to 512 digital channels, mixed signal instruments and the memory test option. Accelerix, a fabless semiconductor company, produces high performance, single chip graphics accelerators with embedded memory for 2-D, 3-D, Video, DVD and MPEG applications in the notebook computer market. The Delta STE will be used for single insertion, multiple die testing at wafer probe and package test of Accelerix's graphics accelerators. Richard White, President and CEO of Accelerix. [www.accelerix.com](http://www.accelerix.com)

**BASIS Communications**, a **Cirrus** spin-off, announced its formation as a provider of Multi-Service Networking ICs for the integration of voice and data. The company will develop and deliver "Network Application Focused Integrated Solutions." The company's RISC based ICs will address the convergence of voice and data over wide area Internet-Centric networks. In the spin-off from Cirrus, BASIS has acquired a portfolio of WAN and ATM products as well as other traditional Serial I/O and Host Based controller products. BASIS will maintain a manufacturing and services business relationship with Cirrus to support the existing portfolio and future products. Michael Shealy, President and CEO, Lloyd Atkinson, senior VP and COO.

Shealy was previously VP and GM of the communications division of Cirrus. Atkinson was formerly the VP of the network access products group in Cirrus' Communications Division. Address: 3100 West Warren Ave. Suite A, Fremont, CA 94538. Tel: 510/668-0107, fax: 510/624-7690, [www.basiscom.com](http://www.basiscom.com)

**Integrated Memory Technologies (IMT)** is believed to be developing Flash memory products. Ching Jenq, President. Address: 2255 Martin Ave., Suite E Santa Clara, CA 94022. Tel: 408/986-1088, Fax: 408/727-8696.

**Interactive Silicon Inc. (ISI)**, a start-up semiconductor IP company in Austin, TX, has appointed **Jim Garrett**, formerly vice chairman and president of Micron Technology, as CEO. ISI was founded in 1998 to license semiconductor IP to semiconductor manufacturers. The company's technology is used to improve bandwidth efficiency, resulting in higher performance, lower power consumption, lower "noise," and lower system and component costs. The company's technology minimizes the amount of data transfer required, reducing memory bandwidth demand which improves performance without having to modify existing application software or software interfaces. The technology improves DRDRAM, SDRAM, EDRAM (embedded DRAM), DDR SDRAM and other types of memory such as FLASH.

ISI's MediaF/X architecture for audio, video, 2D/3D graphics and memory control is comprised of Interactive Media Core(s) that embed in consumer ICs working with industry standard CPUs. MediaF/X reduces system cost and improves performance by combining media acceleration with memory control and by reducing host bandwidth requirements for media operations. Austin Ventures and Rambus participated in the company's first round of financing, completed in June 1998. Tom Dye, founder, president and CTO. Tel: 512/502-0299, fax: 512/502-9065, [www.interactivesi.com](http://www.interactivesi.com)

**MediaQ** was founded in May 1997 to "deliver systems solutions in silicon enabling a wide range of consumer electronic appliances to connect to information, entertainment and communication networks." Private investors have financed the company to date. MediaQ is seeking \$5 - \$10 million in additional financing in this quarter.

MediaQ develops highly integrated silicon solutions that accelerate the development of prod-

Market	11/97	10/98	11/98	Y-to-Y	M-to-M
Americas	4.0	3.6	3.7	-7	2
Europe	2.7	2.6	2.8	3	7
Japan	2.7	2.1	2.3	-16	7
Asia Pacific	2.7	2.5	2.6	-4	5
Total	12.1	10.9	11.4	-6	5

Source: SIA

Month	Shipments	Bookings	BK-to-BL
July 98	1,112	718	0.65
Aug. 98	1012	572	0.57
Sept. 98	846	481	0.57
Oct. 98 (final)	852	638	0.75
Nov. 98 (revised)	932	781	0.84
Dec. 98 (prelim)	924	872	0.94

Source: SEMI

Radar Scope .....	1
Startup Profiles .....	2
People .....	11
IPOs & Equity Placements .....	12
Mergers & Acquisitions .....	12
Business & Financials .....	13
Licensing & Partnerships .....	14
Market Research .....	15
Emerging Applications .....	16
New Products .....	17
Design Wins .....	21
Stock Charts .....	21
Company Financials .....	22
Company Rankings .....	23

## Radar Scope

(Continued from page 1)

ucts for the consumer electronic appliance marketplace. The company's products provide application-specific processing power to devices including micro-notebooks, consumer Internet appliances, client computing devices, and smart telephones. The company has a strategic partnership with Hitachi. MediaQ is also a Microsoft Windows CE Preferred Provider. Windows CE, consumer electronic appliances, S3 founders... If we had to guess, we'd say that MediaQ is developing graphics chips for "Jupiterish" devices. We'll see... Sales channels are being implemented now. Additional details are expected in late March.

Ramesh Singh, president, CEO and co-founder (formerly GM of the Home Products Division at S3)

Ignatius Tjandrasuwita, VP of engineering and co-founder (formerly director of engineering for mobile products at S3)

Sunder Velamuri, VP of sales and marketing and co-founder (formerly established the portable products group at S3)

Brian Davis, dir. of marketing (formerly oversaw technology and business development opportunities for digital set-top boxes at Rockwell Sem.)

3303 Octavius Drive  
Santa Clara, California 95054  
Tel: 408/588-0080  
Fax: 408/588-0084  
www.mediaQ.com

**NUWAVE Technologies** (NASDAQ: WAVE), a provider of video enhancement technology, has concluded the design phase for conversion of its NUWAVE video processor technology into an ASIC. **The Engineering Consortium (TEC)**, a fabless semiconductor and designer of low voltage ICs specializing in mixed signal ASICs, contracted by NUWAVE, has deliver the design files to **ZMD**, the foundry for the device. The NUWAVE Video Processor (NVP) ASIC enhancement technology manipulates video signals with precise digital control. Additional technology included in the NVP ASIC provides for proprietary preset software controls which allow the user or content provider to easily manipulate the amount and type of improvement required for viewing particular types of video

content (i.e., news, drama, sports, animation, etc.). *NUWAVE may license the technology to semiconductor manufacturers as well.* Production in the Spring. NUWAVE was founded in 1995. Gerald Zarin, President and CEO. www.nuwav.com

**Sapphire Design Automation** was recently launched to develop "electrically correct" physical design solutions for DSM chip design. Sapphire's mission is "to address the emerging EDA market segment between logic synthesis and place & route tools by taking an innovative new approach to solving the timing, power, and signal integrity problems associated with deep sub-micron semiconductor technology." The company received \$1.5 million in initial funding from a group of private investors including Bechtolsheim and Andrew Yang. Sapphire's founders are Shashank Goel, president and CEO, Dr. Steven McCormick, VP of engineering, and Nagesh Shirali, director of product development. Sapphire's management team also includes Kevin Walsh, VP of marketing, who joins the company from Avant!

Sapphire's initial target audience is high-end ASIC and customer-owned tooling (COT) EDA users - estimated at more than \$100 million and growing at 20 to 40% annually. Sapphire's software will help define a new "virtual prototyping" market adjacent to Synopsys' installed base of Design Compiler users, which it projects to be worth more than \$350 million when mature. Sapphire's "electrically correct" approach addresses the need to accurately account for delay, cross talk, power consumption, resistive voltage drops, and reliability as part of the DSM design process. Beta testing now. The company plans to formally introduce its products in March.

2310 Walsh Ave.  
Santa Clara, Ca 95051  
Tel: 408/970-0110  
fax: 408/970-0660  
www.sdai.com ■

## Startup Profiles

### C-Port

C-Port was founded in Nov. 1997 to "radically improve the networking industry's ability to develop, deploy, and provision the communications services for the 21<sup>st</sup> century." The company's goal is to "enable network services in Internet time." The company has raised \$8 million in first round financing from Charles River Ventures, Bessemer Venture Partners and Benchmark Capital. Substantial second round financing will be raised in the first half of '99. The company has 55 employees.

We have seen company after company role out ASIC-based networking platforms, only to redesign them from scratch or acquire another company just to get a new ASIC platform for each technology transition. Communications companies are squeezed between numerous conflicting demands such as ever increasing performance, more functionality, faster time-to-market, lower cost, new and ever changing standards, simpler management and more. Software solutions, such as the traditional slow Cisco 7500 router, can't keep up with today's performance requirements. ASIC-based hardware solutions are inflexible, costly, and simply a finger in the dyke. What's need is an entirely new platform, which C-Port calls "Communications Ware."

C-Port's Communications Ware concept is a hierarchical open communications platform. At the lowest layer are the physical interfaces: Ethernet, T1/E1, OC-3, etc. Successive layers include the Communications Engine or Digital Communication Processors (DCPs), Communication Interface or Communications Programming Interface (CPI in C-Port's lingo), Communications Component Software (CCS) consisting of pre-written functions such as SARs, and finally Communications Application Solutions (CAS) such as a L2/3 Switch. The last ingredient is the Communications Development Environment (CDE) which provides a unified design and development environment. The design environment consists of compilers, debuggers, simulators and support that enhance vendor productivity. C-Port's system simulator is orders of magnitude faster than a Verilog simulator yet is cycle accurate, enabling rapid modeling of system behav-

ior. When HP closed its Chelmsford tools development center, much of the world-class team was hired by C-Port.

C-Port is developing a family of Digital Communication Processors (DCPs), full-custom, fully programmable micro-multi-processors optimized for communications applications. The CPI provides a stable set of communications APIs that maintain software compatibility across generations of DCPs. A library of Communications Components such as IP Packet Forward, ATM SAR, HDLC Switch, and Packet over SONET will be provided. The CPI will enable 3<sup>rd</sup> party providers to develop components as well. Rev. 3 of the CPI has already been shipped to several OEMs. At the Application level C-Port will deliver a set of functional communications solutions such as L2/3 Gigabit Ethernet switch, ATM Cell Switch, IP/ATM Switch that OEMs can use as a foundation for developing value-added solutions. Third party suppliers can also deliver application level solutions as well as additional development tools.

C-Port's platform will enable developers to role out successive generations of products without "fork-lift" redesigns. OEMs will be able to incrementally tailor their products for new standards, applications, features and performance requirements. C-Port is not revealing specific architectural or product details yet. However, the processor achieves 3000 MIPS (whatever that means in communications terms), full-duplex aggregate bandwidth of 5Gbps, and will sustain wire-speed OC-12 performance. The processor has a multi-processor architecture and consist of typical base-line instructions coupled with high level communications-centric instructions. It is designed to operate in a multi-processing environment, such as a processor per line card, across a high-performance fabric.

We've been touting the network processor concept for some time now. It appears painfully obvious to us. General-purpose processors don't cut it and ASICs are an exorbitantly expensive undertaking in terms of cost, time, and resources. The packet- and cell-processing world needs its own network-centric processor, just as the signal processing world has DSPs. However, few companies have made any noise in this area. Competitors include Softcom, MMC, Sitera, Tsquare, and possibly Xaqt, and Maverick. However none of these solutions offer a full

custom, open, universal communications platform. Each one addresses an aspect of the problem and offers a step in the right direction, but we think none can be claim to be the DSP of the networking world. While we need to see specific product details for us to proclaim C-Port the holy-grail, we can say that they understand the problem and appear to have the most comprehensive vision for what's required. C-Port has a powerful team consisting of full-custom micro-processor experts, network systems architects, and software tools developers. If anyone can do it they can. We look forward to product details.

Dr. Laurence Walker, CEO (formerly VP/GM of Nwtwork Division and Alpha Semiconductor Group at Digital)

Tom Brightman (cofounder of Cyrix and MediaGX architecture. Also a TMS320 architect)

Dave Husak, CTO (founding engineer at Synernetics and CoreBuilder architect at 3Com)

Clint Ramsay, VP, Marketing  
1 High St.

N. Andover, MA 01845

Tel: 978/974-9317, Fax: 978/974-9489

www.cportcorp.com

## Cognitive Designs

CDI was founded by Scott Finley in 1992 to develop high-performance cryptographic chips. The company provides standard chips and proprietary design consulting services. CDI has 1 employee – Scott! He believes he has designed more cryptographic chips than anyone in the industry has – 8 designs in silicon and 3 cores. He has worked at LSI Logic, Ultron Labs, and VLSI Technology and claims that many of the cryptographic chips on the market are his designs.

For the first few years, CDI provided contract design services. Recently, CDI introduced a family of general-purpose cryptographic chips that offer cost-effective bulk encryption and authentication using a variety of algorithms. Standard cryptographic products include the CDI 2000 Triple-Key Data Encryption Standard (TDES) processor, CDI 2050 TDES and MISTY1 Processor with DMA, CDI 2100 TDES and SKIP-JACK Processor with DMA and PCI, and the CDI 3000 TDES, SHA-1, MD-5 processor with DMA and PCI. The CDI 2000 and 2050 are avail. now, the CDI 2100 and 3000 will be avail. in

Q1 and Q2 respectively. Eval boards are available for all products.

Cryptographic Cores for Triple-Key DES (44-, 88- or 176 Mbps), MISTY1 (264 Mbps), SKIP-JACK (64 Mbps), and Authentication (SHA-1, MD5 – 210Mbps) are available as well. Misc. cores include Dual-Channel DMA Controller, 64-bit Random Number Generator and a Target/Master PCI Interface.

Triple DES uses the single-key DES algorithm three times (3 x 56 bits = 168 bits) for every data block. MISTY1 is a secret-key cryptographic algorithm developed by Mitsubishi. MISTY1 is designed to provide greater security than DES or Triple-Key DES especially for linear and differential cryptoanalysis. The 128-bit key size significantly reduces the success of brute-force key searches as well. An international patent (PCT/JP96/02154) is pending for MISTY. SKIP-JACK is a secret-key cryptographic algorithm developed by the National Security Agency (NSA). It uses an 80-bit key and is designed to provide greater security than single-key DES.

The CDI 2000 Hardware Encryption Processor uses the Triple-Key Data Encryption Standard (triple DES) to provide hardware encryption and message authentication. The device is capable of triple-key DES encryption at 88 million bps in any 64-bit mode of operation. Faster DES cores that achieve 176 Mbps will appear in future chips. It contains a built-in 64-bit Random Number Generator to supply new key and initial vector values. The device is targeted at network suppliers, computer peripherals and other embedded systems.

It provides four key registers and two initial vector registers, and supports ANSI x3.106 modes of operation in one, eight, and 64-bit block sizes. The CDI 2000 supports numerous security and reliability features, including bus parity checking and tamper detection. System diagnostics are supported by a built-in Monte-Carlo Test command. The device supports 5V or 3.3V operation and can be clocked at 0 to 33 MHz. It features an activity monitor that shifts the device into low power standby mode as well. Scott believes that the CDI2000 is the fastest and least expensive chip on the market. It is \$10 in volume.

## Startup Profiles

(Continued from page 3)

Competitors include hifn, VLSI Technology, in house solutions, and several chips developed by security companies. However, Scott believes that most other offerings are expensive and slow. He believes that a high performance solution with a low price point will enable triple DES cryptographic chips to proliferate in new high volume markets. An American ASIC company fabricates the devices.

Scott Finley, President and founder,

RSFinley@aol.com

295 Princeton-Hightstown Rd., Suite 11-242  
West Windsor, NJ 08512

Tel 609/638-7691, Fax 609/897-1011

www.cognitive-designs.com

## Imsys

Imsys was established in the fall of 1992 by Stefan Blixt, Anders Grad'n, and Christian Blixt. Imsys is owned entirely by the majority of its employees, however addition capital may be sought in the future. Imsys has 7 employees, 3 contractors, and 10+ engineers at 3 business partners working full-time on projects related to its GP1000 processor.

Imsys develops processors for high-volume embedded controller products. The company offers microcontroller components, software development tools, and reference designs. The processors are optimized for high-speed real-time control and are also efficient at executing Java, having JVM bytecodes as one of their native instruction sets. High-level functions can be programmed in Java while performance-critical functions can be coded in assembler or highly efficient microcode – cool.

Imsys believes that Java, with its established means of automatic transfer and installation of software, is an ideal language for applications that require rapid development, high-level complex control, high volume, and low cost. Because the Imsys processor has a microcoded JVM, it executes Java rapidly and without using much memory. Flexible microcode and other architectural features make it an efficient low-level ma-

chine for high performance real-time applications as well.

The Imsys GP1000 is a microprocessor with special features for Java as well as for low-level control of I/O signals and data-intensive applications such as image processing. The processor switches between 3 different personalities, i.e. microcode sets: When executing Java, the GP1000's native instruction set is JVM bytecodes. Special microcodes support garbage collection and thread scheduling. A second instruction set for 8-bit and 32-bit data is available for functions that are hardware-dependent or not suitable for being programmed in a high-level language. The third personality is the micro-machine, which executes wide microinstructions containing many different fields governing all details of the processor hardware. A "control microprogram" controls many autonomous actions of the machine and allocates time for the different personalities and tasks.

Data-intensive processes such as document scanning, compression, and decompression can be entirely programmed in microcode. Imsys has microcoded functions for scanning, image enhancement, image buffering, compression / decompression (of continuous tone and bi-level images), and halftoning. Imsys can develop customer specific microcode and is also planning on developing a higher-level language, which can directly produce microcode. The micro-machine can operate on data in almost every cycle, and can access resources not available on higher levels, such as resources normally found in DSP processors.

The device has 4 DMA channels, with a total capacity of 33 MBytes per sec, 3 general purpose 8-bit I/O ports, 8-level priority interrupt system, multiple register sets, sleep mode, watchdog function, real-time clock, timers, and an on-chip oscillator and PLL. The device interfaces directly to up to 128 MB of external DRAM. It is fabricated in a 0.35u process and operates at 66.7 MHz at 3.3V. Power consumption is only 350 mW, with a low 8  $\mu$ W in standby mode. A development system and controller board are available, which run on Windows 95/NT. The GP1000 and development boards have been produced. Controller boards for two different color printers have been built.

The processor core is very small because microcode ROM is much denser than random logic gates. A new ROM-based microcode version contains much of the microcode needed for the execution of most Java bytecodes. The new version will be able to boot from a Multi Media Card (MMC) flash card. Future versions will continue to reduce power and increase clock speeds. Embedded DRAM will be incorporated when the design is shrunk from 0.35u to 0.25u. Designs with multiple processor per chip are also envisioned.

Imsys recently signed a license agreement with Array Printers AB in Gothenburg, Sweden. Array will use the GP1000 processor in printer controller solutions. Ericsson is the foundry partner and will market the technology as well. Clean Bean has been formed by Imsys to establish a sales organization for Java-based embedded control applications. Astrosoft Ltd. (in St. Petersburg) is a software development partner and has developed a C/C++ compiler for GP1000.

Although Sun's processors execute Java, they don't target the same applications as the GP1000. Sun's processor consume about 10x as much power as the GP1000 and is significantly larger even though it is fabricated in a finer line process. Java executes faster on the microJava because many bytecodes are executed by dedicated hardware. However, the GP1000 is a real-time multiprocessing embedded microcontroller and has some DSP features. It can produce half-toned pages to a laser printer at a rate of more than 10 million pixels per second, far beyond Sun processor's capabilities. Imsys has a battery-operated Java demonstrator unit in design.

This is a pretty cool device – it spans the complete programming range from nightmarish microcode to the proclaimed Java panacea.

Lars-Erik Nordell, chairman (cofounder of Innovativ Vision AB and managing director of its subsidiary DocEye AB, the leading supplier of Document Image Processing systems in Sweden)

Stefan Blixt, managing director,  
stefan@imsys.se (cofounder and chairman of Versal AB, a computer terminal system company)

Roger Sundman is responsible for Clean Bean

Ynglingavägen 3  
s-175 77 Järfälla Sweden  
Tel: 46-0-8-58039980, Fax: 46-0-8-58039055  
www.imsys.se

## Ionas A/S

IONAS (Integrated Optical Network Components A/S) was established in Jan. 1997 as a spin-off from NKT Research Center specializing in the design and manufacture of integrated optical components and DFB fiber lasers for multi-wavelength telecom networks. IONAS belongs to the Danish NKT group of companies and is a sister company to GIGA. Its products are based on more than 5 years of research performed at the NKT Research Center and the Mikroelektronik Center at the Technical University of Denmark aimed at developing advanced integrated optical components. The collaboration was concluded by the end of '96 and a large part of the know-how and personnel was transferred to IONAS. IONAS has about 20 employees. The company continues to collaborate with MIC.

The company was founded with starting capital of DKK 25 million (approx. US\$4M) and is currently a subsidiary of I.C. Holding A/S, whose shareholders consist of NKT Holding A/S and venture capital companies, Lønmodtagernes Dyrtdsfond, Dansk Kapitalanlæg A/S and A/S Dansk Erhvervsinvestering. NKT has a 63.25% holding in IONAS, each of the other shareholders have a 12.25% interest. I.C. Holding is also the parent of Giga A/S, which manufactures ICs for the telecom market. Giga recorded a turnover of DKK 53 million (approx. US\$8.3 million) and a pre-tax profit of DKK 8 million (US\$1.3 million) in 1995 and experienced substantial growth in '96. The board members are currently discussing additional capital funding for IONAS.

IONAS develops Optical Integrated Products based on Silica-on-Silicon technology. The technology is a combination of Plasma Enhanced Chemical Vapor Deposition (PECVD) for the formation of the silica layers and Refractive Ion Etching for the creation of the waveguide patterns. Products include both fiber optic and integrated optical components including DFB Fiber Lasers, Fiber Bragg Gratings, and Planar Waveguides.

The main fiber product is DFB fiber LASERS based on Er-doped fiber and UV written Bragg gratings. The fiber LASERS are typically pumped by a semiconductor LASER operating at 1480 nm. The short length of the DFB laser consumes a fraction of the pump power. The remaining power can be used to pump an additional section of Er-doped fiber, enabling output powers of several tens of milliwatts.

The DFB fiber LASERS offer excellent spectral properties utilizing a single polarization operation mode. The LASERS feature a Signal to Noise ratio of 60 dB min and a very narrow line width in the range of 15kHz. IONAS can customize the center frequency and output power to individual specifications. IONAS can provide both single- and multi-wavelength LASERS. The multi-wavelength LASERS feature exceptional stability of the wavelengths relative to each other – very important in WDM networks for which the LASER would be an ideal source in test and measuring equipment.

In April '98, IONAS introduced an ultra-narrow linewidth DFB fiber laser with a linewidth of less than 1 kHz. Combined with a 60 dB SNR, the laser will allow for extreme precision in sensor applications as well as other high-precision measuring techniques. The laser is manufactured by inducing a precisely chosen fiber Bragg grating in the core of an Erbium-doped fiber, which provides internal feedback. Combined with a unique packaging technique it yields a very narrow linewidth. The laser package is 100x100x10 mm and comes with a pump input port and a signal output port. Any center wavelength in the 1520-1585 nm bandwidth can be produced.

In September IONAS introduced a single mode, narrow-linewidth DFB fiber laser operating at 1  $\mu$ m. The high purity wavelength having a laser linewidth of less than 500 kHz can be customer specified between 1.01  $\mu$ m and 1.08  $\mu$ m. The laser requires pumping by a 980 nm diode. It can replace bulky solid state lasers and eliminate coupling loss to optical fiber since the laser is inherently inside the optical fiber. Output power levels can reach 20 mW, Signal to Noise ratio is 60 dB minimum.

In October 1997, IONAS licensed Bragg grating patents from United Technologies Research Center. Under the terms of the agreement, IO-

NAS is fully licensed to manufacture Bragg gratings and sell them worldwide.

Ionas manufacturers reflective type fiber Bragg gratings for dense WDM systems. The products reflect a specific wavelength while transmitting all others and are designed to customized specifications. Narrowband or broadband fiber Bragg gratings are targeted at sensor applications. The center wavelength of fiber Bragg gratings is sensitive to strain, pressure, and temperature (via the thermo-optic effect), and can thus be used as sensors for these parameters. Grating parameters such as center wavelength, reflection / transmission level and bandwidth are designed to customized specifications as well.

Ionas can also develop custom integrated optical circuits, optical add/drop multiplexers, N x N thermo-optic switches, and electrically-adjustable attenuators.

The total marked size for planar waveguide devices is forecasted to be more than US\$4 billion in year 2000. Competitors include Piri, and Kymata amongst others. Most competitive activity comes from internal efforts in large companies such as Lucent, Nortel, and Hitachi. IONAS believes that its PECVD based technology produces superior uniformity control of refractive index and layer deposition on 5-inch wafers. Passive planar waveguide devices are in production now. Active planar waveguide functionality will be integrated during 1999. Customers include major telecom companies worldwide. Ionas has a direct OEM based sales force.

Lars Ronn, Managing Director and VP, Sales and Marketing (formerly in charge of technical and market operations in Denmark for Hitachi Europe)  
Dr Lars U.A. Andersen, Process expert  
Dr. Kevin Malone, Process Expert  
CAT, building 347  
DK-2800 Lyngby, Denmark  
Tel: 45-45-25-6400, Fax: 45-45-25-6405  
www.ionas.dk

## ITRAN

ITRAN Communications was founded in Sept. 1996 to develop power line modem ICs. The company has raised \$1.3 million from Melnick Ventures and Argoquest and is seeking an addi-

## Startup Profiles

(Continued from page 5)

tional \$1 - \$2 million now. ITRAN has 17 employees.

ITRAN has developed several power line modem chips operating at speeds of 10Mbps, 1.5Mbps, 50kbps and 7kbps. ITRAN's home networking and residential access solutions include the 1.5Mbps ITM1 and the compatible 10Mbps ITM10 power line modems. ITRAN also offers the 50kbps IT5000 and the extremely robust 7kbps IT800 for home automation and utility service markets. The ITM1 physical layer is designed for seamless integration with a number of micro controllers, including Ethernet, 802.11 (wireless) and Token ring MACs.

The power line is an extremely difficult communications medium, characterized by several unpredictable and strong interferences including Additive White Gaussian Noise (AWGN), spikes, bursts, colored noise, and Continuous Wave (CW) interference. Power-line communications channels are also corrupted by fast fading, have non-flat frequency response, and unpredictable jamming. ITRAN claims that its initial chip families achieve extremely high performance at a fraction of the cost of existing power line communication chips. The solution is based on a patent pending technology known as Differential Code Shift Keying (DCSK). DCSK modulation is a non-conventional spread spectrum system, providing high speed and reliability with minimal silicon complexity. ITRAN has filed patent applications for its DCSK technique and believes that it is sufficiently complex to present a high technological barrier to potential imitators. The ITM1 and ITM10 represent additional patentable IP as well.

The ITM1 power line modem delivers 1.5 Mbps of speed over residential power lines and is directly compatible with Ethernet, 802.11 and IP protocols. The device is a 30k-40k gate mixed signal physical layer ASIC and requires just a few, low cost discreet components. No information is exchanged a priori between transmitter and receiver, making the component highly efficient for ad hoc networks. The ITM1 supports CSMA with Collision Detection and a 4-20Mhz transmission range with easy modification to other bands. The device is claimed to be the most reliable high bit rate powerline com-

munication chip. The ITM10 operates at 10Mbps and is downward compatible with the ITM1. The ITM10 employs proprietary and patentable turbo-equalizing CDMA with interleaving and convolutional coding. It operates in the 5Mhz to 15Mhz frequency range.

The IT5000 Power Line Network Interface Controller is a low cost, 50Kbps CEBus compatible implementation of ITRAN's DCSK technology. IT5000 devices can communicate with each other up to 8x faster (50 kbps) than the CEBus standard rate (6.6 kbps). IT5000 ICs communicate with other CEBus standard compliant transceivers on the network at the usual CEBus standard speed. Target applications include voice based control applications over residential power lines. The 8Kbps IT800 employs DCSK modulation to enable extremely robust power line communications. With its high robustness to AWGN, pulses, CW interference, and high levels of spectral distortion, the IT800 is claimed to be significantly more reliable than other power line ICs. The IT800 is targeted at robust device control, home automation, Automatic Meter Reading (AMR), security and other high reliability applications.

ITRAN will introduce the ITM1, IT800 and IT5000 modems beginning in Q3 '99. The ITM10 is scheduled to ship in Q4 2000. Future development plans include integrated Ethernet and USB MAC layers, ASSPs for voice, audio, residential access and meter reading applications, and phone Line and RF chips using DCSK.

ITRAN will sell standard silicon products. ITRAN also plans to selectively license its physical layer designs to semiconductor companies that are leading gateway players, such as Intel and Broadcom, that don't compete against ITRAN in the sales of physical layer silicon to the home network "spokes". ITRAN is also forming a power line networking Special In-

dustry Group aiming at de facto standardization of its physical layer devices, the ITM1 and ITM10. ITRAN will seek partners in networking, PC, consumer electronics, cable modem, xDSL, and residential gateway companies. ITRAN is currently in negotiations with several potential strategic partners.

Numerous companies are entering the home networking market. RF and phoneline solutions abound as well. As we discussed in the Enikia profile last month, our favorite is powerline since it's ubiquitous and cheaper than RF to date. ITRAN has compared its solution with several competitors with the results indicated below. What's missing is a comparison with other leading edge solutions, such as Enikia's. While Enikia appears to have taken a DSP approach, ITRAN relies on a very smart physical layer, which it claims will have a lower cost structure.

In addition to the obvious home networking and meter reading markets, high-speed powerline networking can enable utilities to deliver broadband services. In March 1998, Nortel and United Utilities formed a joint venture company, NOR.WEB, to market Digital PowerLine technology. Digital PowerLine, which was developed jointly by Nortel and Norweb Communications, part of United Utilities PLC, enables data communications to be transmitted over electricity power distribution networks at speeds of more than 1 Mbps. Check out the Norweb site ([www.nor.webdpl.com](http://www.nor.webdpl.com)) to learn more about Nor.web's plans.

A power line communications chip contract design was completed and licensed in April 1997. Evaluations are under way at several American and European public networking companies. Several firms in the US Home Automation and Networking industry have agreed to be beta sites for the ITM1 PHYlayer chip. In Feb. '98 ITRAN announced a strategic relation

### Competitive Landscape According to ITRAN

<u>Company</u>	<u>Modulation Technique</u>	<u>Bit Rate</u>	<u>Est. Modem Manf. Cost</u>	<u>Est. External Components Cost</u>
ITRAN	DCSK	1.5Mbps	\$3	\$0.50
Intellon	OFDM	1Mbps	\$7	\$3
Intellogis	FSK	350Kbps	\$5	\$2
ANI	Spread Spectrum	100Kbps	\$7-\$10	\$2
Echelon	FSK	10Kbps	Multi-chip soln	Multi-chip soln

with Home Automated Living, a developer of voice control home automation software. HAL has agreed to purchase \$1.37 million of IT5000 chips in one year. HAL is collaborating with ITRAN and the NASA design firm Jackson and Tull to produce automated wall switches that will carry voice commands to the PC via existing home power lines. Jackson and Tull is designing automated wall switches for HAL with tiny microphones and speakers which will enable users to talk to their PCs from any room in the house, hands free, where the switch is installed. The new switch will also have sensors for motion and temperature control and will be CEBus compatible. The switch is expected to be priced at under \$100. Pretty cool.

ITRAN will establish a direct sales force and will partner with distributors outside of the US and Europe prior to product release in Q3 '99. Foundry negotiations are under way.

Avner Matmor, President (formerly VP Operations at Qualitau, a Santa Clara, CA based provider of stress testing equipment to the semiconductor industry)  
 Dr. Dan Raphaeli, Chief Scientist (a researcher at Tel Aviv University in the Electrical Engineering Systems Department)  
 Eitan Einwohner, Director, Business Development and N. American Marketing Manager  
 15 Yehoshua Hatzoref Street  
 P.O. BOX 844  
 Beersheva 84106 Israel  
 Tel: 972-7-6235281, Fax: 972-7-6231246  
 www.itrancomm.com

P.O. Box 460425  
 San Francisco, CA 94146 USA  
 Tel: 415/643-6240, Fax: 415/449 3502

## Opticom ASA

Opticom ASA, a Norwegian based R&D Company, was founded in 1994 to develop all-organic opto-electronic memory and processing system. Shares in Opticom are quoted on the Oslo Stock Exchange SMB List. The Company has 29 employees and is engaged in 39 research collaborations world-wide.

Opticom is developing all-organic memory and data-processing system. All-organic means that the memory medium and entire read/write sys-

tem are made exclusively from organic materials. The control circuitry, including the electrodes, are made exclusively from organic compounds and printed directly onto the organic storage elements. No silicon chips or external components are required to perform read/write/erase functions. Opticom's use of organic or polymer materials combined with its multi-layer system design and architecture offers massive storage capacity and ultra-fast access and transfer rates. It allows for a solid state, non-volatile system that is small, robust, has very low power consumption and lends itself to Reel-to-Reel manufacturing techniques.

The conducting properties of polymer were discovered in 1975 and the first polymer transistor was developed in 1989. During the past several years Opticom has made a number of advances in organic memory systems as indicated below.

Opticom's technology has been refined over the past few years, reflecting the progress in various fields of research including material composition issues (chemical modeling and engineering of novel molecular structures), electronic circuitry design, memory architectures, printing and manufacturing technologies. Three distinct memory systems have been developed and tested, of which the single layer Polymer Memory system represents the latest iteration and preferred platform for future memory products.

The first iteration, Microlens Focusing, was developed between 1993 and 1995, using polymer microlenses as focusing elements incorporated directly into the storage medium. The second system, Proximity focusing, removed the focusing elements in order to achieve thinner system layers, and thus a larger capacity. In 1997 the Polymer Memory system was developed. A single, thin layer of organic material sandwiched between two electrodes replaced the emitter/memory film/detector sandwich. A memory cell is spontaneously created by applying current at a certain voltage to a top and bottom electrode. The organic material is modified where the electrodes cross. By changing the voltage level, information can be written, read or erased. No active circuitry is required within each memory cell.

This is significantly simpler than conventional memories, which require from 1 to 6 transistors per cell. It offers the potential for much

smaller cells (0.1 – 0.4 $\mu$ m<sup>2</sup>) and thus higher storage capacity. No silicon chips are used, not even for the control circuitry, which has several advantages such as Reel-to-Reel manufacturing for continuously processing a substrate that is wound from one roll to another. This procedure is much more efficient than the wafer processing used to fabricate ICs or the discrete production of CD and hard disk systems. The RTR approach may yield square meters of memory and processing devices per second. A typical roll size may be up to 1.25 meters wide, which will result in a production capacity of several square meters per second.

A fully functioning Polymer Memory system can be built on a surface area of just a few square microns, with a total thickness of less than 10 microns. The organic materials used in the Polymer Memory system can be coated or deposited from solution onto flexible substrates. Adding a new memory layer simply means coating another layer on top of a previous one. The electronic circuitry is then printed directly onto each such layer. With a total thickness of less than 0.5 microns per layer, thousands of memory layers will fit within the form factor of a thin "credit" card.

Read, write and erase operations can be accomplished in a massively parallel manner. A typical memory area consisting of one million cells covers less than 0.5 mm<sup>2</sup>. The memory areas can be accessed in parallel in every memory layer. The combined effect is a very high data transfer rate (all layers can be addressed individually), and very fast random access to large data words (vertical word architecture).

The Polymer Memory system is non-volatile. Less than a picojoule of energy is required to read, write or erase one bit of information, several orders of magnitude lower than rotating disk and tape systems. The power consumption is so small that the embedded battery capacity is expected to last for the whole system lifetime (8 - 10 years).

During 1997 Opticom has been focused on improving the system architecture, optimizing its rewritable organic materials, developing high mobility, reel-to-reel (RTR) compatible semiconductor materials, fabricating the control circuitry on flexible substrates, developing high resolution printing techniques, and developing a RTR processing pilot line. The technology for

## Startup Profiles

(Continued from page 7)

building full scale WORM (write-once-read-many) devices has been developed to a stage where it is ready for implementation. Two classes of erasable films have also been developed to a level where fully operating, large capacity devices can be built. Opticom has successfully built and tested a 1 Mbit memory array based on a newly developed all electrical, switchable memory architecture.

Opticom has developed a hybrid polymer/CMOS process that is based on existing silicon CMOS chip fabrication techniques, enabling first generation devices to be fabricated using existing silicon manufacturing equipment and foundries. A design has been developed that allows up to 5 memory layers to be included as part of a 6-metal 0.25u CMOS process.

Opticom and its partners have developed, tested, and demonstrated organic based components required to build ROM/WORM and erasable memory systems. Pre-programmed read-only demonstrators have been developed, tested, and demonstrated using rigid and flexible substrates. Access and data transfer speeds have been tested for erasable films. The basic logic design for a fully erasable memory system has been completed, including simulations of all performance parameters. Opticom has also developed the design for an all-organic parallel processing system, essentially an all-organic microprocessor.

In 1997, the company secured its first license agreement via the establishment of the US\$15 million Eidopt As joint venture with Eidos plc. The Eidopt project uses a multiple of the basic 1-Mbit memory array for a hybrid silicon/polymer ROM computer games card which will offer access and data transfer rates more than 1000x better than present CD and DVD applications. Opticom, on behalf of Eidopt joint venture, has contracted an independent chip design house and foundry to build the first fully packaged hybrid chip for delivery in '99.

Opticom has 39 joint venture research partners including Lucent and AMP. In 1998 Opticom launched a marketing effort to license its technology world-wide. Opticom has identified a

number of potential partners in specific product areas and is in discussions with a number of partners, which may lead to the signing of additional licensing agreements.

Thomas Fussell, Chairman  
 Hans Gude Gudesen, Research Director and founder  
 Robert Keith, Managing Director  
 Per Erik Nordal, PhD, senior research manager for opto-electronic systems  
 Johan Carlsson, PhD, Physicist in electronic materials  
 Göran Gustafsson, PhD, Physicist in polymer physics and microelectronics  
 Magnus Berggren, PhD, Physicist in polymer physics and optics  
 Brynsveien 3B  
 N-0667 OSLO Norway  
 Tel: +47-22-97-09-30, Fax: +47-22-97-09-35  
 www.opticomasa.com

## RC MODULE

RC MODULE, a Russian electronics company, develops image processing and neural network software, embedded computers (part of the computer system on the International Space Station), and ASICs including the NeuroMatrix NM6403 Processor. RC Module has been financed via contract design projects and is currently seeking about \$500K from western investors. The company had planned to achieve revenues of US\$4 million in 1998, but due to the financial crisis only expects to achieve about US\$1 million. The company has about 100 employees.

The NM6403 is a high performance microprocessor with a super scalar architecture. It integrates a 32/64-bit RISC core and 1-64 bit DSP co-processor (patent pending) to support matrix calculations with elements of variable bit length. The device has 2 identical 64-bit programmable memory interfaces and 2 communication ports, hardware compatible with the TMS320Cx comm port. The NM6403 achieves 1200 MMAC at a 50MHz clock rate and 8-bit

operands. It is designed in 0.5um CMOS, with a 3.3V power supply and a BGA256 package. The NM603 will start shipping in March '99.

The NM6404 next-generation version will have the same RISC and VECTOR cores as the NM603 in addition to the following new features: 2-Mbits internal memory, access to internal memory from neighborhood, 8-, 16-, 32-, 64-bit external memory support, SDRAM support, FFT support, JTAG port, PLLs and power management, and 200MHz clock in 0.24u CMOS.

A full suite of development tools are available including a C++ compiler, assembler, linker, emulator, source level debugger, object files librarian, load and exchange library, run-time libraries, and Cadence compatible behavioral Verilog model.

The NM6403 is available as a discrete IC, TIM module, or board level VME and PCI product. The PCI board is available in single or dual processor configurations. The NeuroMatrix NM6404 Processor will also be available as a chip or PCI board.

Competitive products include digital VLSI Neuroprocessors such as the Philips Lneuro, Inova N64000, or Siemens MA-16, neural network accelerator cards such as BrainMaker accelerators and the Nestor Ni1000, and fixed-point DSPs such as the Analog Devises ADSP-2100, Motorola DSP561xx and TI 320C54x. RC MODULE believes that the NM6403 provides superior speed vs. precision trade-offs than other alternatives.

The NM6403 has achieved 4071 clock cycles for 256 point FFT. TI's C62x DSP performs the same task in 4225 clock cycles. The device achieves Alpha 500 MHz performance with Haramard Transform at 40 MHz clock rate.

The company plans to ship silicon and is interested in licensing the design as well. The NM6403 is fabricated at Samsung. A wafer

Benchmarks:	Sobel Transform	FFT	Harmard-Walsh	Forward pagation
Frame size:	256-point	21 step,	1024 layers,	
Processor	384x288 bytes	32-bit data	Init.data, 5-bit	neurons/layer
Pentium II, 300	N/A	N/A	2.58 sec	N/A
Pentium 200	21 frame/sec	N/A	2.80 sec	N/A
TMS320C40, 50Mhz	6.8 frame/sec	0.46 ms	N/A	N/A
NM6403, 40Mhz	37 frame/sec	0.08 ms	0.45 sec	1.54 sec



foundry has not been selected yet for the NM6404. The company has several Russian and German customers and has also provided the NeuroMatrix 2-CPU PCI Board to HiNT (Fremont, CA) for evaluation. The NM6403 is RC Module's first chip design. The company uses Cadence and Synopsys design tools and is prepared to make high-end chips for external customers. RC Module is a certified Fujitsu Design Center in Russia and has a long-standing partnership with Samsung. The company has several reps worldwide including Alternative Solutions in France.

Given the Russian financial crisis and our media-influenced Western bias, we questioned RC Module's viability, considering the jeopardy involved in designing in a high-end sole-source device like the NM6403. Dimitir said Samsung produces the processor and joint-marketing negotiations are under way. If necessary, he would sign a contract to license the design in the event that "MODULE" Research Centre becomes insolvent. The NM6403/4 appears to be very interesting and RC MODULE clearly has significant intellectual property – worth exploring.

Ioury Borissov, Managing Director  
 Michael Jafrakov, Scientific Director  
 Dmitri Fomine, ASIC Section Manager,  
 fomin@module.vympel.msk.ru

"MODULE" Research Centre  
 3 Eight March 4Th Street  
 Box: 166, Moscow, 125190 Russia  
 Tel: 7 095 152-9335, Fax: 7 095 152-4661  
 www.module.vympel.msk.ru

## Seagull Semiconductor

Seagull was founded in June 1998 to develop high integration and high performance system-on-a-chip products. Seagull's mission is "to develop and market best-in-class VLSI ICs for high growth markets." The founders, private investors, and fees from a Siemens project have financed the company. Siemens is not an investor, although it might choose to invest in the future. If so, Seagull would like to keep Siemens' ownership under 15%. Seagull will seek about \$2 - \$3 million in mid-'99. The company has 20 engineers.

The company is focused on 2 major markets: Communications and Computer Telephony Integration, both of which can use Seagull's combined RISC/DSP expertise. Seagull offers cus-

tomization and integration capabilities for ASSP chips and IP products. Seagull focuses on combining RISC and DSP on a single chip to handle control tasks and signal processing respectively. Seagull can provide expertise in system partitioning of software vs. hardware and programable vs. fixed-function hardware. Seagull's expertise includes complex IP such as RISC and DSP, communication modules such as Ethernet, T1/E1, and modems, analog cells such as PLLs, DACs, and ADCs, and system elements such as DMA, Caches, ICU, and UARTs.

Seagull has close cooperation with Siemens with ongoing large projects. In July 1998, Seagull signed an agreement with Siemens to start a new TriCore Processor project. In Dec. 1998, **Siemens** and **Seagull** signed an agreement to extend their partnership on the development of cores and modules for TriCore licensees and customers. Seagull has started to develop additional IP for Siemens's TriCore, a single-core 32-bit microcontroller-DSP architecture optimized for real-time embedded systems.

Siemens is currently the only customer. Negotiations are in progress with several other potential customers about projects in areas such as DVD. The company claims to have the resources to handle multiple projects.

Seagull plans to market standard products in 1-2 years. The company has recently hired a software expert for real time algorithms and protocols for control and DSP. Seagull will expand this capability in the future to provide complete solutions. Siemens is the foundry for the first product. TSMC will be the foundry for future products. Seagull plans to establish a rep sales force worldwide.

Gigy Baror, President and founder (Gigy participated in the architecture definition of National's 32532, Ross' Danlite Sparc, AMD's 29000, and Siemens' Tricore processors)

Zeev Bikowsky, CEO and acting VP of sales and marketing (formerly VP of core technology business unit at DSP Group)  
 Amnon Yeger, VP of R&D and founder (has managed large design teams at Motorola, ACRI, EMC and ROSS)

1 Maskit St., P.O. Box 12580  
 Herzelia Pituah, Israel, 46733  
 Tel: 972-9-9516150, Fax: 972-9-9516153

US contact:

Zohar Peleg, director of product marketing and on-site coordinator for the Siemens project (formerly applications manager and system architect for PC products at National)

P.O. Box 2128  
 Cupertino, CA 95015-2128  
 E-mail: zoharp@seagull.co.il  
 Tel: 408/792-3322

## Sybarus Technologies

Sybarus was founded to develop SONET ICs and software. Its mission is "to be unsurpassed in the ability to design and apply SONET based communications technologies." The company designs ASICs, ASSPs and cores for datacom and telecom companies, and firmware and software for SONET/SDH interfaces and networks. Sybarus is developing high capacity OC-48/192 products for DWDM networks including Packet-Over-SONET (POS), SDH-Lite (SDH-L) and direct Data-Over-Fiber (DOF) products.

Sybarus specializes in complete IC design, verification, and support services for the Telecom and Datacom community. Using its IP, Sybarus can develop ICs for SONET/SDH Section/Line Termination, STS/STM Path Termination and Payload Alignment, VT/TU Path Termination and Payload Alignment, STS and VT Cross Connects, DS1/E1 Framers and Mappers, DS3/E3 Framers and Mappers, ATM Cell Delineation and Processing, Cell/Packet Switch Fabrics, Segmentation And Reassembly, and HDLC (POS & FR) Processing.

Sybarus has also developed several toolsets, which claim to maximize code reuse, ensure compliance to industry specifications (for SONET, SDH, ATM, POS, PDH), and minimize design and verification effort.

Verilog/VHDL PreProcessor (VPP) is a productivity enhancement tool for IC designers. It enables design abstraction using simple extensions to standard Verilog/VHDL, which results in a reduction of code size (approx. 1/3 the number of lines of code), an increase in productivity (average 5x) in design and maintenance, and increased reusability through parametrization of code (for example STS-N pointer processor, where N is set to 1,3,12,48,192 at compile time). VPP is currently in use by several hundred designers and is the standard coding language at

## Startup Profiles

(Continued from page 9)

several sites within large Telecom and Datacom equipment companies.

Sybarus is bringing to market its internal communications testbench for SONET/SDH/ATM/POS. The tool enhances the ASIC development process by reducing the verification effort while increasing the level of conformance testing. Manipulating and monitoring APS bytes, payload pointers, Packet streams, etc., can be as simple as a few easy-to-use commands, due to the internal protocol engines within the testbench. Automation of test cases simplifies circuit debugging and regression testing. The tool will be available this summer.

Sybarus is developing an integrated SONET/SDH software package for Network Interface Cards. It provides configuration management, fault management, state management, performance monitoring and maintenance management in a standards compliant and fully tested package.

The company is keeping very quiet and will not disclose any other details. Although the software products are nice, we're guessing that the focus is IC development. Stay tuned for additional details.

16 Fitzgerald Road, Third Floor  
Nepean, Ontario K2H 8R6 Canada  
Tel: 613/829-0040, Fax: 613/829-1186  
www.sybarus.com

## TeraGen

TeraGen was founded by Donald Sollars and Terry Gannon in Feb. 1997 to develop a new class of microprocessor called a Thread Processing Unit for embedded applications. TeraGen raised \$2 million in first round funding from InterWest Partners and Sequoia Capital Partners and just closed a \$6.6 million round from the same V/Cs. The company has about 17 employees.

The company is targeting the embedded processor market, estimated to be \$12 billion in 1998, growing to \$25 billion in 2001. In the year 2000, the average automobile is expected to have about 35 processors and the average home may contain several hundred.

Current architectures are based on a single process model and are instruction set specific. Ever increasing performance demands lead to large die sizes and poor cost / performance tradeoffs. Hardware fixed-function peripherals are "bolted" around the core processor further increasing die size. New peripherals require new silicon.

TeraGen has invented a new architecture called a "Thread Processor" which is used to implement all types of embedded processors, including microcontrollers, DSPs, and peripheral controllers. Thread Processing breaks down a complex task into multiple, independent processes that can be performed concurrently. The thread processor can process *any* instruction set – including those in use by existing microcontrollers and DSPs. The architecture also allows a single device to implement combinations of dissimilar instruction sets. TeraGen claims that its technology will lower cost, increase performance, and reduce application design cycles, while protecting existing software investments. The architecture also permits the functionality of peripheral controllers to be incorporated into the thread processor as internal software threads, rather than hardware, somewhat akin to Scenix's "virtual peripherals" approach.

Incoming software instructions as well as on-chip-generated "soft peripheral" instructions are broken down into parallel sequences of simpler instructions called "threads." Soft-peripherals and a specific ISA are contained in ROM-based thread processes. Incoming threads are scheduled, by a Scheduler, for execution on one or more "micro-thread engines" – highly optimized, small, on-chip processing elements. Thread processors may be built to process threads in parallel, using one or more simultaneous-acting, independent micro-thread engines.

TeraGen believes that the combination of an "open instruction set architecture" with "soft peripherals" is ideally suited for the creation of next generation embedded processors. It enables one chip to perform the tasks formerly allocated to several and preserves the application vendor's software investment. The architecture is also claimed to be scaleable and extremely efficient in its use of chip area.

TeraGen claims that its Thread Processor technology will permit the rapid design of a broad range of embedded processors, from simple 8-bit controllers to sophisticated 16-, 24- and 32-bit RISC processors and DSPs. The Thread Processor enables any device to be made fully compatible with pre-existing instruction set architectures permitting existing microcontrollers and DSPs to be replaced with significantly enhanced versions, which can utilize pre-existing software.

The technology is initially being targeted at four areas: Enhanced performance versions of popular microcontrollers and DSPs, integrated controllers which combine the functionality of microcontrollers and DSPs, customized controllers with enhanced instruction sets, application-specific features or custom peripherals, and application-specific devices such as protocol-translation chips.

The Thread Processor accommodates any existing ISA, protecting software investments. Thread-based peripherals enable easy customization of peripherals and co-processing functions. The technology is highly efficient and is 90% ROM, RAM and Data Path, maximizing circuit density. TeraGen believes that it will lead to a 10:1 cost / performance improvement compared to current technologies.

TeraGen's partners will begin production of the first commercial products built with the technology in the first half of '99. In Oct. '98, ZiLOG started shipping the Z8E000, a \$0.39 (@500Ku) 8-bit OTP microcontroller. The Z8E000, the newest member of the Z8Plus family, was designed in cooperation with TeraGen and uses some of TeraGen's concepts. TeraGen will initially license its technology to processor companies. It will develop standard ICs in phase 2 of its strategy.

Donald Sollars, Chairman  
George Alexy, President and CEO (formerly chief product marketing officer at Cirrus)  
Terry Gannon, VP of Engineering and Operations  
2075 Landings Dr.  
Mountain View, CA 94043  
Tel: 650/404-8080  
Fax: 650/404-8090  
www.tera-gen.com ■

# People

**Alliance** appointed **David Eichler**, formerly VP of Finance and Chief Accounting Officer for Adobe, as VP of Finance and Administration and CFO. Alliance also named **Brad Perkins**, formerly VP and General Counsel for Mission West Properties, as VP and General Counsel. N. Damodar Reddy, CEO and President. [www.alsc.com](http://www.alsc.com)

**AMCC** announced that **Joel Holliday** intends to retire as CFO. A search is in process for his successor. Holliday will remain with the company for an unspecified time to ensure a smooth transition. Dave Rickey, president and CEO.

**Aspec Technology** announced an executive management restructuring strategy with **Dr. Conrad Dell'Oca** now serving exclusively as Chairman. **Douglas Klint**, currently VP, General Counsel, has been appointed acting President and CEO. **Michael O'Malley** has been appointed CFO and acting COO. O'Malley has served as a consultant to the Company since November. [www.aspec.com](http://www.aspec.com)

**Dense-Pac** named **Ted Bruce**, formerly senior manager of North America Manufacturing for Toshiba America, as president. **Richard Daddamo**, who has served as interim president and CEO since August, will remain CEO and has joined the board. [www.dense-pac.com](http://www.dense-pac.com)

**ESS** announced that **Matt Fong** has joined the company as a Board member and will also be employed as Advisor to the President. Fong was most recently California's State Treasurer and the Republican Nominee for the US Senate (CA). Fred Chan, President and CEO. [www.esstech.com](http://www.esstech.com)

**Fujitsu Microelectronics** named **Takashi Yabu** as VP and GM of the Gresham Manufacturing Division. He is in charge of the production of 64M SDRAMs. Yabu was most recently GM of the Technology Development Division of Fujitsu Ltd.'s LSI Group. Yabu replaced **Jun Nakano**, who has returned to Japan to work in the Electronic Devices Group. Fujitsu will also add a logic product line this year to increase the factory's efficiencies. Yuji "Gene" Ezura, president and CEO. [www.fujitsumicro.com](http://www.fujitsumicro.com)

**Micro Linear** announced that **Arthur Stabnow** has retired as Chairman, CEO and President for health reasons. **David Gellatly** has been elected to serve as CEO and President. Since 1982 Gellatly has been the principal of New

Technology Marketing, a high technology marketing consulting company.

**MMC Networks** appointed **Fred Berkowitz**, former director of engineering at Silicon Graphics, as VP of engineering. **Alex Joffe**, formerly VP of engineering, has been promoted to executive VP and CTO of MMC Networks. Amos Wilnai, chairman and interim CEO.

**Mosel Vitelic** appointed **Mark Grant**, formerly director of Intellectual Property and chief IP strategist at National, as VP and General Counsel. [www.moselvitelic.com](http://www.moselvitelic.com)

**National** named **Jean-Louis Bories** as executive VP and GM of its Cyrix subsidiary. Bories has been senior VP of the company's Core Technology Group since 1997. The company also announced the formation of an Information Appliance group to further its strategy of developing system-on-a-chip solutions for the information access market. The group will be headed by **Michael Polacek**, who was named VP, reporting to Bories. National also named Senior VP **Kevin McDonough** as its second National Fellow. [www.national.com](http://www.national.com)

**Peregrine** promoted **Milt Miller** from Director of Sales to VP of Sales. Peregrine also named **Douglas Mathews**, formerly VP of Endpoint and Mobile Systems at ITRON, as VP of Design and **Steve Whelan**, formerly VP, Marketing & Sales for Torrey Communications, as VP Business Development. All 3 report to Stavo Prodromou, president and CEO.

**Scenix** appointed **Bulent Celebi**, formerly VP/GM of the power mgmt., temperature sensor, amplifier and aerospace product lines at Analog Devices, as president and CEO. Celebi has served on Scenix's board since the company's formation and was involved in its product definition and strategy. Steve Leung, president and CEO since co-founding the company, remains as chairman. [www.scenix.com](http://www.scenix.com)

**SMSC** promoted **George Houseweart** to Senior VP and General Counsel, from Senior VP of Law and Intellectual Property. Paul Richman, Chairman and CEO. [www.smsc.com](http://www.smsc.com)

**Synopsys** appointed **Andy Bryant, Sr.** VP and CFO of Intel, and **Dr. Sass Somekh**, a member of the Office of the President at Applied Materials, to its Board. Dr. Aart de Geus, Chairman and CEO. [www.synopsys.com](http://www.synopsys.com)

**SwitchCore**, a developer of single-chip switches and wire-speed routers, appointed **Nitish**

**Amin** as director of business development. Prior to joining SwitchCore, Amin held key sales positions at several semiconductor suppliers including Digital, Intel and National. Per Anderson, president of SwitchCore AB. Tel: 408/995-3850, Fax: 408/995-3858, [www.switchcore.com](http://www.switchcore.com)

**Three-Five Systems** (NYSE: TFS) announced the resignation of **Vincent Hren**, President, CEO and Director. Three Five has retained Korn/Ferry International to complete the search for a replacement. **David Buchanan**, Chairman, will assume the additional duties of President and CEO on an interim basis. Three-Five has created the new position of CTO, which it expects to fill during the first half of 1999. **Charles Rahrig**, VP of Engineering and **Dan Schott**, VP of R&D will report to this new senior executive position. Three-Five is working on LCaD (Liquid Crystal active Drive) and LCiD (Liquid Crystal intense Display) technologies, as well as LCoS (Liquid Crystal on Silicon) microdisplays. Lawrence Kagemann, VP of Operations. [www.threefive.com](http://www.threefive.com)

**Unitrode** announced that **Cosmo Trapani**, Executive VP and CFO, will be leaving the Company to pursue entrepreneurial interests in a move that has been planned for some time. Robert Richardson, Chairman and CEO. [www.unitrode.com](http://www.unitrode.com)

**Vantis** promoted **Andy Pease** to VP of Worldwide Sales and named his successor, **Mark Lunsford** to the position of VP of North America Sales. Pease now reports to Rich Forte, CEO. Vantis also appointed **Vincent Tortolano**, formerly associate general counsel and director of Technology Law for AMD, as VP and general counsel. **Rick Crowley**, formerly National's VP and Corporate Controller, has been appointed VP and CFO. [www.vantis.com](http://www.vantis.com)

**Veridicom**, a Lucent spin-off and provider of silicon-based fingerprint authentication solutions, appointed **Michael D'Amour** as CEO, replacing former CEO and founder **Tom Rowley**, who remains at Veridicom and provides strategic counsel on security projects. D'Amour was formerly the president and founder of D'Amour & Associates, a consulting firm specializing in assisting high technology companies with business plan development, executive management and funding. D'Amour also founded Quickturn Design Systems. [www.veridicom.com](http://www.veridicom.com)

**Virtual Silicon Technology**, a provider of semiconductor libraries and physical design components, named **Dr. Terry Thomas**, formerly

## People

(Continued from page 11)

managing director of strategic alliances and design systems for Nortel Semiconductors, as VP of strategic alliances. He also serves on the board of directors of the Virtual Socket Interface Alliance (VSIA). Taylor Scanlon, president and CEO. [www.virtual-silicon.com](http://www.virtual-silicon.com)

**ZiLOG** appointed **Michael Burger**, formerly VP of WW marketing and sales at QuickLogic, as Senior VP of Worldwide Sales. ZiLOG also appointed **Dr. Gianpaolo Spadini**, formerly VP of technology development at Microchip, as VP of technology development. Curtis Crawford, President and CEO. [www.zilog.com](http://www.zilog.com) ■

## IPOs & Equity Deals

**Aptix** has received \$11.5 million in a private placement led by Partech International and IN-VESCO Private Capital. All previous investors also participated in the round. Aptix provides a solution for prototyping complete systems and system-on-chip designs. The System Explorer is a reprogrammable system for integration of software with custom logic, off-the-shelf components and hard or soft IP. Aptix has experienced an annual average growth rate of over 50% and has shipped over 400 System Explorer products. In its most recent quarter, Aptix received orders for new systems from Ericsson, Rockwell Collins, TRW, iTEX, Fujitsu, iReady, Nokia and Siemens Wireless, amongst others. Amr Mohsen, president and CEO. Tel: 408/428-6200, Fax: 408/944-0646, [www.apitx.com](http://www.apitx.com)

**NVIDIA** (Nasdaq: NVDA) announced the IPO of 3.5 million shares of common stock at \$12 per share. Morgan Stanley Dean Witter, H&Q and Prudential managed the offering. The company originally filed on March 6, 1998. [www.nvidia.com](http://www.nvidia.com)

**Sage** has raised more than \$6 million to date. Sage's largest investor in '98, the InveStar Venture Fund has provided \$3 million in funding. Sage announced sales increases of 400% over fiscal '98 compared to '97. Demand from customers such as Taiwan-based monitor manufacturer LiteOn Technologies has fueled Sage's growth as new LCD monitors based on Sage technology have gone into production. The Cheetah II ASIC automatically adjusts the video image to match the full size of the screen, the panel's resolution and refresh rate, the spectrum of available colors, and high quality scal-

ing, with both horizontal and vertical interpolation. Chandra Reddy, president and CEO. [www.sageinc.com](http://www.sageinc.com)

**XEMICS** has received 7.8M Swiss francs (about US\$5.7M) from five new shareholders who now hold 44% of the total shares. The other 56% remaining with CSEM in Switzerland. XEMICS specializes in ultra low-power ICs and was established 15 months ago as a spin-off from CSEM. A second round of financing is anticipated at the end of '99. In 1998, its first year of operation, the company had revenues of 19M Swiss francs (approx. US\$14M). Thomas Hinderling, Chairman, Roland Heer, CEO. ■

## Mergers and Acquisitions

**Amkor** (NASDAQ:AMKR) has signed an agreement with **Anam Semiconductor** to acquire Anam's K4 semiconductor packaging and test facility located in Kwangju, Korea for up to \$600 million in cash, plus the assumption of up to \$7 million in liabilities. K4 is a state-of-the-art semiconductor packaging and test facility with over one million square feet of manufacturing and support space. Currently, it is producing advanced semiconductor packages including PBGA, MicroBGA, SuperBGA and TSOP. [www.amkor.com](http://www.amkor.com)

**Atmel** has signed a non-binding memorandum of understanding to acquire the Smart Information Transfer (SIT) business of **Motorola SPS**. The proposed transaction does not affect Motorola's other smart card-related businesses, such as its Worldwide Smartcard Solutions Division (WSSD). Atmel claims that the acquisition will position it as the world's 3<sup>rd</sup> largest smart card IC supplier. George Perlegos, Atmel's president and CEO. Billy Edwards, corporate VP and director, Strategic Management and Planning, Motorola SPS.

**Broadcom** has signed a definitive agreement to acquire **Maverick Networks** (see 7/98 issue), a San Jose, Calif.-based company developing multi-layer switching ICs. Maverick's technology delivers Layer 3 Fast and Gigabit Ethernet switching and packet classification features to the workgroup switch market. Broadcom will issue 864,200 shares of its Class B Common Stock in exchange for all shares of Maverick Stock, about \$127 million based on a current price of \$147 for Broadcom. Maverick's technology is claimed to deliver line-speed, Layer 2-3 switching in hardware with a programmable real-time packet processor operat-

ing up through Layer 7. **Alliance** owned approx. 28.4% of the total outstanding shares of Maverick. In Feb. '98, Alliance entered into investment and technology license agreements with Maverick to assist them in developing ICs for multi-layer network switches. Dr. Henry Nicholas III, Broadcom's President and CEO. G. Venkatesh, Maverick's President and CEO.

**Cadence** and **Quickturn** have amended their merger agreement to increase from \$14 to \$15 the amount of Cadence stock that Quickturn stockholders will receive for each Quickturn share. Jack Harding, president and CEO of Cadence, Keith Lobo, Quickturn president and CEO. [www.cadence.com](http://www.cadence.com), [www.quickturn.com](http://www.quickturn.com)

**Cadence** has agreed to acquire **Design Acceleration (DAI)** of San Jose, a supplier of design automation technology used in system-on-chip design, for about \$27 million in cash and Cadence common stock. The 40 DAI employees will join the Cadence organization. DAI offers design analysis products that enhance designer productivity through a flexible, intuitive analysis environment for design debug. DAI's product portfolio includes DAI Signalscan for waveform viewing, DAI Coverscan for code coverage analysis, and DAI Comparescan for simulation comparisons and rules-based analysis. DAI was founded in 1993. More than 400 corporations including Broadcom, Compaq, Cyrix, Hitachi, HP, IBM, Intel, Motorola, National, Nortel, Silicon Graphics, Sony, Sun, and TI have purchased DAI products. Glenn Abood, VP for design and verification products at Cadence. Dean Drako, president and CEO of DAI. [www.designacc.com](http://www.designacc.com), [www.cadence.com](http://www.cadence.com)

**Cypress** and **IC WORKS** signed a definitive agreement for ICW to merge with Cypress. ICW, a provider of system timing generation ICs, had average quarterly revenues of about \$17.6 million and net income of about \$2.7 million during the last three quarters of fiscal '99. The agreement provides for Cypress to issue 13.7 million shares in exchange for all outstanding stock and options of ICW. T.J. Rodgers, Cypress president and CEO, Ilbok Lee, IC WORKS president and CEO. [www.cypress.com](http://www.cypress.com), [www.icworks.com](http://www.icworks.com)

**C-Cube** has acquired communication technology, patents, and personnel from **TV/Com International**, part of the **Mindport Group**, located in San Diego. The acquisition provides C-Cube with strategic communication technologies for interactive cable and satellite digital set-top boxes. The new products and the exist-

ing products will enable C-Cube to deliver a complete digital set-top solution. Umesh Padval, president, C-Cube Semi Division. [www.c-cube.com](http://www.c-cube.com), [www.mindport.com](http://www.mindport.com)

**Davicom** has acquired Ethernet switch technology from **NETiO Technologies**. NETiO has built a core technology for the implementation of Ethernet and Fast Ethernet switching semiconductors. NETiO was founded in 1997 to develop 10/100 Mbps and Gigabit Ethernet LAN switching products. Ting Herh, Chairman and CEO of Davicom. David Lin, President and CEO of NETiO. [www.davicom8.com](http://www.davicom8.com)

The **Dii Group** announced that **Orbit**, its wholly owned subsidiary, has signed a definitive agreement to sell its wafer fab to **Supertex**, a Sunnyvale, Calif., mixed-signal semiconductor manufacturer. As part of the transaction, Supertex has guaranteed Orbit a multi-year supply of wafers that utilize the specialized processes run in the facility. Dii expects that the sale will result in about a \$13-\$14 million after-tax, non-recurring, noncash charge in the fourth quarter and anticipates the deal will be cash positive – contributing about \$5 million. Ronald Budacz, chairman and CEO of the Dii Group, Ronald Snyder, President of Orbit, Dr. Henry Pao, President and CEO of Supertex. [www.diiigroup.com](http://www.diiigroup.com)

**Genesis Microchip** (Nasdaq: GNSSF) has signed a definitive agreement to merge with privately held **Paradise Electronics** of San Jose, CA, strengthening its position as the leading supplier of ICs for flat panel displays. Under the terms of the merger, 4.5 million shares of Genesis common stock will be exchanged for all outstanding shares and options of Paradise. Alexander Lushtak and another Paradise board member will join the Genesis board. Paradise president Jeff Diamond will serve as Genesis's executive VP. Founded in 1996, Paradise develops highly integrated mixed-mode ICs for the flat panel monitor market. Single-chip flat-panel solutions are the way to go, and the Paradise acquisition provides Genesis with a quick jumpstart into the market. Paul Russo, Genesis chairman and CEO, Stephen Solari, Genesis president and COO, Alexander Lushtak, chairman of Paradise. [www.genesis-microchip.com](http://www.genesis-microchip.com)

**ISD**, which will retain its name and logo, has become part of **Winbond's** San Jose-based subsidiary, Winbond Electronics of America (WECA). **David Angel** plans to step down as CEO in 1999. Y.C. Chiao, CEO of Winbond. [www.winbond.com.tw](http://www.winbond.com.tw), [www.isd.com](http://www.isd.com)

**PC-TEL** purchased the Technology Alliance Group (**TAG**) from **General DataComm** (GDC) of Middlebury, Conn., for an undisclosed amount. PC-TEL will operate the group as its new Communications Systems Division, dedicated to developing and licensing modem, remote access and other telecom IP. The new division will be headed by **Frank Reo**, VP of business development and licensing at PC-TEL. All 20 employees of TAG will join the Communications Systems Division and become PC-TEL employees. PC-TEL acquired 34 patents and applications in the telecom area and gained additional presence on the ITU standards-setting committee. The patent portfolio includes eight V.34 and nine V.90 modem patents. The portfolio acquired from TAG, in combination with PC-TEL's 12 patents and applications in host signal processing, gives PC-TEL the ability to license key IP, further strengthening the company's market position and expanding its business model by creating an additional profit center. The VisionQuest 2000 analyst group predicts that sales of HSP modems will grow 150% in '99 from '98. TAG was created as a division of GDC in 1998 to take advantage of GDC's IP. Peter Chen, president and CEO. [www.pctel.com](http://www.pctel.com)

**STMicroelectronics** has completed its acquisition of the Peripheral Technology Solutions (PTS) group from **Adapttec**. The Company announced the acquisition on Nov. 25, 1998. Aldo Romano, Corporate VP, Telecom Peripheral and Automotive Groups. [www.st.com](http://www.st.com)

**TI** has entered into an agreement to acquire **Butterfly VLSI** (see 1/99 profile), a developer of RF wireless technology targeting communications in a range of up to 100 meters. Butterfly, with sites in Tel Aviv, Israel, and Santa Clara, California, develops low cost chipsets that enable RF wireless communications in the 900 MHz and 2.4 GHz frequency bands. The company employs about 60 people, primarily in engineering, who will become part of TI and operate under the TI name. The purchase price was about \$50 million. Gilles Delfassy, TI VP and manager of the Wireless Communications business unit. Gideon Barak, Butterfly's CEO. [www.butterfly.com](http://www.butterfly.com)

**Vitesse** has agreed to acquire **Serano Systems** for common stock. Serano is a provider of enclosure- and platform-management solutions for fibre channel, and SCSI server and storage subsystems using industry-standard protocols (e.g. SES, SAF-TE and IPMI). Serano's semiconduc-

tors and software building blocks provide a reliable and easy-to-use means for storage area networks (SANs) to easily control configuration, monitor status and isolate faults in complex storage systems. The acquisition of Serano strengthens Vitesse's role in fibre channel SAN solutions and provides one-stop shopping for its high-end JBOD customers. Serano has 13 employees and is located in Colorado Springs, Colo. Michael Millhollan, GM of the data communications division. Joe Edens, president and CEO of Serano. [www.vitesse.com](http://www.vitesse.com)

**Xilinx** has completed the purchase of a number of software assets that it was negotiating to buy. The software includes PLSynthesizer, a synthesis tool, ABEL, the most widely used high-level description language for PLDs, and Design Navigator, a team-based, web-enabled software environment that unites design entry, synthesis, place 'n route and simulation functions. ■

## Business & Financials

**Conexant Systems** (Nasdaq: CNXT) has started operations as the largest independent company focused exclusively on semiconductors for communications. The company's stock has begun regular trading on the NASDAQ using the symbol CNXT. Rockwell shareholders of record at the close of business on Dec. 11, 1998 received one share of Conexant for every two shares of Rockwell stock. The American Stock Exchange will also begin trading options of Conexant (QXN). Conexant was created from Rockwell's spin-off of its \$1.2 billion Semiconductor business to Rockwell shareowners.

The new company is headed by **Dwight Decker**, who was previously president of Rockwell Semiconductor Systems and is now chairman and CEO of Conexant. Conexant's management team includes: **Moiz Beguwala**, senior VP/GM for the Wireless Communications Division, **F. Matthew Rhodes**, senior VP/GM of the Personal Computing Division, **Anthony D'Augustine**, senior VP/GM for the Digital Infotainment Division, **Kevin Strong**, senior VP/GM of the Personal Imaging Division, and **Raouf Halim**, senior VP/GM for the Network Access Division. Conexant begins operations with nearly 6,300 employees, including approx. 2,100 located at its Newport Beach headquarters. [www.conexant.com](http://www.conexant.com)

**Echelon** (Nasdaq: ELON) has been notified by **Motorola** that Motorola will not supply the Neuron Chip family of processors after Janu-

## Business & Financials

(Continued from page 13)

ary 31, 2001. Motorola is a stockholder of Echelon and will continue to seek synergistic uses of LonWorks networks and acceptance of the LonWorks system on conventional application specific embedded processors. Toshiba also produces Echelon's Neuron chips. Bertrand Cambou, senior VP, Motorola Networking and Computing Systems Group. Ken Oshman, president and CEO of Echelon. [www.echelon.com](http://www.echelon.com)

**IBM** was awarded the most U.S. patents in 1998, for the 6<sup>th</sup> consecutive year, shattering the previous record by more than 40%. The company received 2,658 U.S. patents in '98, 934 more patents than in '97, and eclipsing the next closest company by 38%. IBM is the first company to receive more than 2,000 U.S. patents in a single year. IBM's 1998 U.S. patent portfolio includes more than 700 software-related patents and over 375 related to network computing. Several dozen patents are directly related to silicon germanium and silicon-on-insulator chip technology. The number of U.S. patents awarded to IBM in the five previous years were 1085 in '93, 1298 in '94, 1383 in '95, 1867 in '96 and 1724 in '97. The company's IP portfolio generates more than \$1 billion annually.

Other companies in the top ten for '98 were Canon with 1925, NEC with 1628, Motorola with 1406, Sony with 1315, Samsung with 1305, Fujitsu with 1190, Toshiba with 1171, Eastman Kodak with 1125, and Hitachi with 1094. IBM's IP Network Site at [www.ibm.com/patents](http://www.ibm.com/patents) offers free access on information for all U.S. patents granted since 1971. Full images of 2.1 million U.S. patents issued since 1974 are available, as well. In October 1998, the site added European Patents and published International Patent applications. Nicholas Donofrio, senior VP, technology and manufacturing.

**ICS** has entered into a definitive agreement under which an investor group comprised of its senior management together with affiliates of Bain Capital and Bear, Stearns & Co. will acquire all of the outstanding shares of ICS at a cash price of \$21.25 per share, approx. \$261 million based on 12.3 million outstanding shares. The transaction was unanimously approved by ICS' Board. Dr. Stav Prodromou, former president and CEO of ICS, opposes the buyout. He believes that the offer is far below the current market valuation for similar fabless mixed-signal chip companies. Prodromou is

currently the president of Peregrine and is trying to oust ICS' board in a proxy battle. The Company has also entered into a definitive agreement to sell IP and engineering hardware and software related to its datacom business to 3Com for about \$16 million in cash. ICS will have certain licensing and technical support rights, and will continue to sell and support its existing and prospective fast Ethernet transceiver product family to current and new customers. Rudolf Gassner, Chairman. [www.icst.com](http://www.icst.com)

**ISSI** has completed the planned additional sale of a portion of its Taiwan subsidiary to a group of private investors. The company sold an additional 6.5% of its holdings for approx. \$4.5 million, after Taiwan withholding taxes. In addition, certain shares were sold to employees of ISSI-Taiwan. As a result of these transactions, ISSI's ownership in the Taiwan company dropped to approx. 42%. ISSI's long-term goal is to have ISSI-Taiwan go public on the Taiwan stock exchange. ISSI originally established the Taiwan subsidiary in 1990 and assumed 100% ownership in 1993. ISSI-Taiwan coordinates manufacturing logistics for ISSI, performs final test on ISSI memory devices, and covers sales and marketing in Asia. Dropping below 50% ownership positions ISSI-Taiwan for a possible public offering in Taiwan in 2000. In Taiwan, a company cannot go public if the total foreign ownership exceeds 50% in the one-year period prior to a public offering. Jimmy Lee, president and CEO. [www.issiusa.com](http://www.issiusa.com)

**NeoMagic** announced that during Nov. '98, it shipped the ten millionth unit of single-chip embedded DRAM multimedia accelerators. NeoMagic has also shipped the one-millionth unit of its newest product, the MagicMedia 256AV multimedia accelerator. Announced in June '98, it is a 256-bit multimedia accelerator with audio, graphics, video and DVD playback capabilities. It integrates a 256-bit graphics accelerator and an AC97-compliant PCI/AGP audio codec with sample-rate conversion and a digital mixer. The 21-million-transistor chip has DVD-playback acceleration with motion compensation and includes 2.5MB of built-in SGRAM. It supports 1024x768 resolution with true color and consumes less than 1 watt. To date the MagicMedia256AV has been incorporated into more than 15 different notebook PCs from Compaq, Dell, Gateway, HP, IBM, Sony, and Toshiba amongst others. For Q3 '98, NeoMagic shipped 48% of the total portable graphics market in terms of units, and achieved 57% of the total portable graphics market in terms

of revenues. Ron Jankov, senior VP and GM of NeoMagic's Multimedia Products Division. [www.neomagic.com](http://www.neomagic.com) ■

## Licensing & Partnerships

**MOSAID** has concluded a worldwide, non-exclusive patent licensing agreement with **Fujitsu Ltd.** Terms were not disclosed. MOSAID currently has over 50 issued patents and more than 100 pending, many relating to DRAMs. This represents MOSAID's first such general patent licensing arrangement. MOSAID granted Fujitsu 'most-favored-licensee' status as part of the agreement, due to the long-term business relationship between the companies and Fujitsu's status as the first licensee. During the negotiations MOSAID was represented by **The Consortium for Technology Licensing, Ltd.**, of Nissequogue, N.Y. MOSAID has engaged The Consortium for Technology Licensing to act as the Company's agent in other discussions that are currently underway with several large semiconductor memory suppliers which MOSAID believes are using its patented technology. George Cwynar, President and CEO, Dan Mathers, Senior VP of MOSAID, and GM of its Semiconductor Division. [www.mosaid.com](http://www.mosaid.com)

**Photobit** and **Tower** are cooperating on CMOS image sensor technology. The firms have been working together for 2 years on custom and off-the-shelf CMOS image sensors. Disclosure of the Tower-Photobit cooperation follows Photobit's announcement of a broad patent covering its camera-on-a-chip technology and the launch of two new CMOS imagers. Nick Doudoumopoulos, president of Photobit, Reuven Marko, Tower's VP of marketing and sales. [www.photobit.com](http://www.photobit.com)

**RF Micro Devices** has expanded its relationship with **IBM** to add access to IBM's Silicon Germanium (SiGe) foundry services. The Company has accelerated its efforts to design RFICs based on IBM's SiGe process and plans to use SiGe for a broad range of custom and standard RFICs. William Pratt, CTO, Jerry Neal, VP of sales and marketing. [www.rfmd.com](http://www.rfmd.com)

**Sound Vision** announced an agreement with **IBM** to work on production-ready digital camera designs for OEMs. The agreement is focused on combining Sound Vision's Clarity 2.0 digital imaging ASIC and software with IBM image sensor chip technology. The Clarity 2.0 ASIC integrates support for LCDs, Kopin's CyberDisplay, Compact Flash, SmartMedia, USB, and RS232, and supports both CCD and CMOS

image sensors. Bob Caspe, founder and Chairman, Ken Torino, dir. of IBM Microelectronics SCM Services. [www.soundvisioninc.com](http://www.soundvisioninc.com)

**SST** and **Acer** have signed a 5-year technology licensing and foundry agreement. SST will license its patented SuperFlash technology to ACER and will receive royalty revenue from ACER for its use of SuperFlash in embedded applications. ACER will manufacture advanced technology products designed by and for SST. SST expects first production shipments from ACER's foundries to take place in the year 2000. SST has previously announced licensing relationships with IBM, Samsung, Sanyo, Seiko-Epson and TSMC. Stan Shih, chairman and CEO of Acer, Bing Yeh, president and CEO of SST, Sohrab Kianian, dir. of technology licensing and bus. development at SST. [www.ssti.com](http://www.ssti.com)

**VM Labs**, creators of the NUON interactive multimedia standard, announced the implementation of new strategic peripherals partnerships based on its new peripherals licensing program. The partners will introduce an assortment of controllers and accessories for NUON-enhanced DVD players and set-top boxes in 1999. These products will allow users to enjoy high performance videogames, educational and reference applications, in addition to standard movie and audio content playable on current systems. Peripheral partners include SC&T International, NYKO Technologies, Imagin.Net, and the Loral Group.

IDC expects DVD player shipments to reach almost 9 million units in the US in 2002. In addition to a powerful set of advanced DVD features, NUON DVD players provide videogames, Internet surfing, and a broad set of family resource applications, with high-quality 3-D graphics. VM Labs has garnered strong support from the DVD industry based on the belief that NUON's DVD capabilities will enable content diversity, educational and entertainment value and Internet connectivity through an all-in-one DVD entertainment center, and therefore increase the appeal of DVD.

The NUON processor replaces the MPEG decoder chip currently found in DVD Players. A full range of NUON peripherals will include a variety of interactive controller devices, as well as an Internet kit to add functions such as Web browsing and e-mail. A NUON enhanced DVD movie disc is Open DVD compatible and will play on any Open DVD player. However, when played on a NUON DVD player all the additional interactive and graphic enhanced features

will become available to the viewer. NUON DVD offers high quality DVD functionality, including a full color user interface, smooth shuttle, special effect trick modes, and programmability for new features. Richard Miller, CEO, Donald Thomas, Jr., Director of Peripheral Licensing and Promotion. [www.vmlabs.com](http://www.vmlabs.com)

**Winbond** has taken a license for the **Rambus** high-bandwidth memory-interface and will incorporate the interface into forthcoming 144M/128M and beyond DRAMs. Sample in Q3, prod. in Q4. Dr. Kuang-Yi Chiu, Executive VP, Allen Roberts, VP/GM of Rambus' Memory Tech. Div. [www.winbond.com.tw](http://www.winbond.com.tw), [www.rambus.com](http://www.rambus.com)

**ZiLOG** and **World CallNET**, a developer of consumer Internet software, announced the launch of email-enabled TVs, which may be priced on a par with standard TVs. WCN's Ultra Thin Client Protocol (UTCP) architecture and software technology has been integrated with ZiLOG's TV controller and embedded modem technologies to enable the rapid development of M@ilTV, a TV system that allows consumers to conduct personal communications through their TVs without the cost of a set-top boxes. WCN's server-based software architecture makes it possible to offer this capability directly inside the TV at no significant premium in terms of the overall cost of the TV set.

The M@ilTV module (designed by WCN and produced by ZiLOG) is designed to be completely self-contained & pre-certified and will

be located completely inside the TV box. Set-up by the consumer will be as easy as connecting the M@ilTV set to a phone socket. ZiLOG and World CallNET have already started a MailTV implementation program with Vestel Corp. of Turkey. Vestel, an OEM TV manufacturer, has substantial market shares in key European countries such as Germany, England and France. Manufacturing arrangements for the new technology within the U.S are also under way. Aydin Koc, Senior VP and

GM of the Home Entertainment Business at ZiLOG. Paul Goodman-Simpson, CEO of World CallNET. [www.mailtv.com](http://www.mailtv.com), [www.zilog.com](http://www.zilog.com) ■

## Market Research

According to **Consumer Electronics Manufacturers Association (CEMA)** President Gary Shapiro, Digital Television (DTV) momentum is building, as evidenced by sales of 13,176 units just weeks after the launch of digital broadcasts on November 1. At least two thirds of all DTV sets sold in 1999 are predicted to be HDTV sets. [www.CESweb.org](http://www.CESweb.org)

According to **Dataquest** 7 of the top 11 vendors saw their worldwide revenue drop by at least 14% in 1998. Intel was one of the few vendors to post positive revenue in 1998, with revenue surpassing \$22.6 billion. The differential between Intel and No. 2 vendor NEC increased with Intel's semiconductor revenue being 2.7 times that of its nearest rival. Philips, STMicroelectronics, and Siemens all increased their ranking, leading to three European vendors in top 10 for the first time. [www.dataquest.com](http://www.dataquest.com)

**Gemplus** has been ranked as the leading worldwide vendor of chip cards on a unit basis in 1997. According to Dataquest chip cards are the highest-volume electronics end product in the world and smart cards constitute the largest and fastest growing segment of this market.

**Top 20 WW Semiconductor Vendors by Revenue Estimates (US\$ Millions)**

1997 Rank	1998 Rank	Company	1997 Revenue	1998 Revenue	'97-'98 Growth (%)
1	1	Intel	21,746	22,675	4.3
2	2	NEC	10,222	8,271	-19.1
3	3	Motorola	8,067	6,918	-14.2
5	4	Toshiba	7,253	6,055	-16.5
4	5	Texas Instruments	7,352	6,000	-18.4
7	6	Samsung	5,856	4,752	-18.9
6	7	Hitachi	6,298	4,649	-26.2
9	8	Philips	4,440	4,502	1.4
10	9	STMicro	4,019	4,300	7.0
12	10	Siemens	3,441	3,866	12.4
8	10	Fujitsu	4,622	3,866	-16.4
11	12	Mitsubishi	3,925	3,733	-4.9
13	13	IBM	3,391	3,245	-4.3
15	14	Lucent	2,762	3,100	12.2
14	15	Matsushita	2,847	2,645	-7.1
18	16	AMD	2,341	2,36	1.0
16	17	National	2,759	2,226	-19.3
17	18	SANYO	2,471	2,225	-10.0
20	19	Rohm	2,053	1,967	-4.2
21	20	Sony	1,974	1,829	-7.3

Source: Dataquest

## Market Research

(Continued from page 15)

Dataquest forecasts a \$6.8 billion worldwide market for chip card by 2002 with a 38% growth rate. Dataquest projects that smart card revenue worldwide will represent 70% of the chip card market by 2002, up from 56% in 1997. Dataquest also forecasts that Japan and the U.S. will be the fastest-growing regions for chip card sales from '97 to 2002, with sales increasing from \$14 million in '97 to \$390 million in 2002 for Japan, and from \$19.5 million to \$532 million for U.S.

Europe had 77% of worldwide chip card revenues in '97. The European market will remain the largest region with 48% of global sales by 2002. The report forecasts that, by 2002, the Asia Pacific will account for 30% of worldwide sales, the Americas (excluding the U.S.) will account for 9% of sales, and the U.S. will account for 8% of sales. The Japanese market is expected to account for 6% of sales by 2002.

Dataquest splits chip cards into 2 categories: smart cards that include embedded microcontrollers, and memory cards that include embedded memory and possibly other logic functions. According to Dataquest, chip cards are evolving from fixed-function microcontrollers into programmable systems, capable of downloading, managing, and running multiple applications. In the future, they will perform essential identification and security functions in computing and Internet access. [www.gemplus.com](http://www.gemplus.com)

According to IDC, home networking products will be among the hottest technology area in 1999. The growth in home offices is seen as a key factor behind vendors' interest in home networking solutions. There are 37 million home office households in the U.S., of which 8 million have more than two PCs. Currently, there are about 910,000 home office households with LANs – representing 71% of the 1.3 million total U.S. households with LANs. By 2002, the number of home office households with local networks is expected to increase to more than 8 million. [www.idc.com](http://www.idc.com)

In-Stat reported that cable modem unit shipments will grow by 60% in 1999. North America drives the cable modem market and will account for more than 50% of cable modem unit shipments through 2003. In 2000, unit shipment growth will increase to 120% as the DOCSIS standard cable modems become widely available at retail in North America. However In-Stat believes that the quick move from DOCSIS 1.0 to DOCSIS 1.1 will cause consumer confusion in North America in '99. Cable modem vendors are expected to have DOCSIS 1.1 modems certified and available on retail shelves in late '99. Cable modem revenues will hit \$800 million in 2003 while the semiconductor dollar opportunity reaches \$250 million in 2003. [www.cahnersinstat.com](http://www.cahnersinstat.com)

Microdesign Resources reported that worldwide shipments of high-end (32-bit and 64-bit) embedded microprocessors grew 37% from the previous year, to almost 250 million units. The volume leader was Motorola's 68K family which includes ColdFire shipments. ARM achieved 5x growth after years of signing licenses. We assume that much of this growth is in the digital cellular market and expect their volumes to continue to climb. Hitachi's SuperH family grew modestly, impacted by Sega's decision to pull its Saturn console (which uses 3 SuperH processors) from North American shelves. Sega's new Dreamcast console only uses one SuperH processor and has not been introduced yet. Intel and AMD each took a third of the embedded x86 market, leaving the last third for National and ST, amongst others.

A survey of nearly 300 networking professionals, recently conducted by Sage Research, finds that most are looking to upgrade their older category 3, category 5 and STP cabling to enhanced category 5, category 6 and fiber optic cabling. 57% will upgrade at least part of their networks within 2 years. Sage projects that fiber, enhanced category 5 and category 6 cabling will replace category 5 cabling as the most common cable types within the next two years. As installation and equipment costs continue to fall, fiber optic cabling is becoming the cabling of choice. [www.sageresearch.com](http://www.sageresearch.com)

According to SEMI, the North American semiconductor equipment industry posted a book-to-bill ratio of 0.94 for December 1998. Three-month

average shipments in Dec. '98 were \$924 million, 1% below the Nov. '98 level, and 41% below the Dec. '97 level. Three-month average bookings increased in Dec. '98 to \$872 million, 12% above the Nov. '98 level, and 44% below the Dec. '97 level. [www.semi.org](http://www.semi.org)

The SIA reported that worldwide semiconductor sales jumped to \$11.38 billion in November, the highest mark since December 1997. A rally in the Japanese and Asia-Pacific markets led total sales to a 5% increase from October. Sales in Japan and the Asia-Pacific climbed 7% and 4.8%, respectively. Chip sales in Europe also soared in November, climbing 7.3% from October. The October-November upswing of 5% is the biggest October-November jump since 1990. [www.semichips.org](http://www.semichips.org) ■

### Total 1998 unit volumes and growth rates

Processor	Units (millions)	CAGR (%)
68K	83	5
MIPS	50	4
ARM	48	400
SuperH	26	10
x86	12	36
i960	9	0
ST20	7	200
PowerPC	5	40
29K	2	-25
MCORE	1	—
SPARC	<1	—
TOTAL	244	37

Source: MicroDesign Resources, 1999

## Emerging Applications

Compaq launched a new line of Presario Internet PCs, which includes desktop models that enable consumers to digitally network their homes using existing phonelines. Compaq's home phoneline networking solution is based on the industry standard set by the Home Phoneline Networking Alliance (HomePNA). Home phoneline networking uses existing in-home phone wiring to connect computers and operates concurrently with any normal telephone service, including high-speed DSL Internet connections.

Compaq is also including WinGate Home 3.0 Internet Sharing Software from Deerfield.com. WinGate allows up to three PCs in the home to share a single Internet connection and is compatible with all types of Internet access (analog, cable, DSL and satellite). The high-end Presario 5670 comes with a home phoneline net-

### U.S. Home Office PC Forecast, 1998 - 2002 (millions)

	1998	1999	2000	2001	2002
Home office	37.3	40.2	43.2	46.5	49.6
Home office w/PC	26.3	29.3	32.4	36.0	39.2
Home office w/multiple PCs	7.8	8.5	9.7	10.7	12.1

Source: IDC



work adapter, a 1.5 Mb Max Digital Modem, a 10 Mbps Ethernet port, and an IEEE-1394 port. The Presario 5600i is available in several configurations, some of which include Ethernet, a home phonenumber network adapter and a 1.5 Mb Max Digital Modem (G.Lite/V.90). Rod Schrock, Senior VP and Group GM, Consumer Products Group. Mike Rubin, Director and GM, Presario Desktop Division. [www.compaq.com](http://www.compaq.com)

**The Double Data Rate Synchronous DRAM (DDR SDRAM)** memory chip standard has received support from 29 manufacturers of enabling technologies in addition to 12 leading DRAM suppliers. These additional 29 companies include makers of chipsets, connectors, clock drivers, modules, and buffers. DDR SDRAM is a new, open memory chip standard developed and approved by JEDEC.

Support components are available from Hitachi, Hyundai, IDT, Micro Linear, Motorola, Pericom, Philips, Sanyo, and T.I. The parts generate differential clocks, provide 2.5V SSTL\_2 compatible voltage sources, and offer buffering for registered modules. The major module makers all have plans to support DDR-based modules. The new high-speed DDR 184-pin module DIMM is supported by Amp and Molex. Via and Opti are developing a DDR chipsets for the PC market. Alpha Processor, Inc. is developing a DDR based chipset to support their processors, and VLSI is developing chipsets for consumer applications. Semiconductor memory companies supporting DDR SDRAM include Fujitsu, Hitachi, Hyundai, IBM, LG, Micron, Mitsubishi, NEC, Samsung, Siemens, Toshiba, and Vanguard. Most are already sampling DDR and all will ship in volume in 1999.

**Philips and British Airways** are conducting a 2-month field trial of Philip's I-CODE smart label RFID technology. British Airways will use this technology to help identify 75,000 suitcases travelling with passengers from Munich, Germany and Manchester, UK to London's Heathrow airport. The trial, which began last month, represents the first large-scale trial to identify airline luggage, using disposable "smart labels" to speed up luggage handling, reduce missing baggage and increase security.

Each "smart bag tag" contains an IC, that can be programmed with detailed information such as the date and time the luggage is checked in, the weight, as well as a unique identification number and the passenger's destination. The I-CODE IC can be placed between two layers of paper, inside the baggage tag currently used by

airlines. The IC is attached to an antenna, which also lies inside the label, and communicates with the scanner by radio signals, from a distance of up to 1.2 meters away. No battery is required inside the label as the I-CODE chip is powered by the radio signal from the scanner. Several smart labels can be scanned simultaneously, speeding up the baggage handling process. The information on smart labels can be re-programmed, or added to, without the need to print and attach a new label. [www.semiconductors.philips.com](http://www.semiconductors.philips.com) ■

## New Products

**ACD** announced a family of Dual-Speed "Super Class" Ethernet Hub Controllers. The ACD300xx family is a 10/100Mbps Ethernet solution that integrates 8-, 12-, 16-, or 24-ports, a high performance, dual-speed hub engine, integrated bridging function, MACs, and Address Resolution Logic (ARL) into a single 3.3V IC. The only external components required are PHYs and ASRAM. The architecture removes the limitation of existing dual-speed hubs that use a single 2-port 10/100 bridge to convert 10 Mbps traffic on one port to 100 Mbps traffic on another port. The ACD300xx family allows every port to simultaneously operate at 10 or 100 Mbps, eliminating congestion on all ports. Prod. now. Prices vary from \$28 for the 8-port device to \$48 for the 24-port device at 10Ku. Jay Deng, president, CEO and co-founder, Brian Gillings, VP of sales, marketing and customer applications. [www.acdcorp.com](http://www.acdcorp.com)

**AMCC** introduced the S2066, CMOS quad-channel transceiver. Each of the S2066's four channels operate at 1.25 Gbps (full duplex) in conformance with IEEE 802.3z Gigabit Ethernet specification. The S2066 is targeted at high-density switching applications such as Ethernet backbones, multi-port Gigabit Ethernet cards, switched networks and data broadcast environments. Production now, \$68 @ 100. Jack Basi, director of marketing for datacom and computer products. [www.amcc.com](http://www.amcc.com)

**AMD** announced availability of the low-power Mobile AMD-K6-2 processor family for notebook computers. With a top speed of 333 MHz, AMD claims to offer the highest speed mobile processor – for now. The Mobile AMD-K6-2, also available at 300- and 266-MHz and is the first PC processor for notebook computing that uses AMD's 3DNow! technology. The K6-2 supports Socket 7 notebooks, as well as Super7 platforms that offer advanced features includ-

ing a high-performance 100-MHz frontside bus and AGP graphics. Mobile Super7 chipset support is available from ALi and VIA. Toshiba's Satellite 2520 uses the 300-MHz Mobile AMD-K6-2 processor. The Mobile AMD-K6-2 operates at a core voltage of 1.8V and dissipates less than 8W running typical applications. AMD-K6-2 processors integrate 9.3-million-transistors and are manufactured on a 0.25u, 5-layer-metal process technology. The 333-, 300- and 266-MHz Mobile AMD-K6-2 processors are \$299, \$187 and \$106 respectively at 1Ku. S. Atiq Raza, AMD co-COO and CTO. [www.amd.com](http://www.amd.com)

**ATI** announced the RAGE XL and RAGE XC general purpose graphic accelerator chips. The new .25u graphics chips provide high-quality, full AGP 2X acceleration and 2D, 3D and video acceleration for corporate computing systems. The RAGE XL integrates a Transmission Minimized Differential Signaling (TMDS) transmitter to support digital flat panels using the P&D, DFP or DDMG standards. TMDS provides a direct digital link from the computer to the flat panel, with no need for D/A and A/D conversion. RAGE XL supports TFT panels resolutions up to 1280x1024.

The RAGE XL and RAGE XC are software compatible with all RAGE PRO designs, and pin compatible with the RAGE 128. For 3D acceleration, the RAGE XL and RAGE XC integrate a 1.2 million triangles/second set up engine. AGP support, including 2X timing, SideBand Addressing and AGP texturing, further reduce CPU and bus bandwidth requirements. The chips have a 4KB on-chip texture cache and support for Gouraud shading, single-pass bi-filtering, and Direct 3D texture lighting, among other 3D features. Motion video acceleration features include hardware DVD decode through Motion Compensation) and IDCT (Inverse Digital Cosign Transformation) functions which provide full frame rate playback of DVD content. Image quality is enhanced through smooth video scaling and 4-tap horizontal and 2-tap vertical filtered scaling techniques. Samples now, production in March. Philip Eisler, director of component marketing. [www.atitech.com](http://www.atitech.com)

**Broadcom** has commenced high-volume shipments of a custom 10/100 BASE-TX Controller IC for **3Com's** Fast EtherLink XL 10/100 PCI NIC. The IC is the first in a family of single-chip controller solutions being developed by the two companies, based on the Broadcom

## New Products

(Continued from page 17)

**Digi-(PHY)** 10/100 Ethernet PHY technology, for the Ethernet NIC and LAN-on-Motherboard (LOM) market. The Digi-(PHY) core architecture has been shipping for over one year in Broadcom's Quad-(PHY) family and has been deployed in over 20 million Ethernet switch and hub ports worldwide. The Digi-(PHY) architecture has been ported to 0.5u and 0.35u single-poly CMOS process and supports both 3.3V and 5V operation. Jim Jones, Director of Marketing of 3Com's LAN Connectivity Division. Kirk Blattman, Director of Engineering for 3Com. Marty Colombatto, VP and GM of Broadcom's Networking Business Unit.

**Broadcom** announced the BCM5218 Octal-(PHY) Transceiver, an 8-port transceiver for the 10/100 Ethernet switch market. It is Broadcom's third successful implementation of integrating eight 10/100BASE-T transceivers into a single chip. The BCM5218 supports both the RMII and SMII interfaces. Samples now, prod. in Q1, \$26 @ 10Ku. [www.broadcom.com](http://www.broadcom.com)

**Burr-Brown** announced the VSP2080, a front-end signal processing IC for CCD digital cameras. The device features correlated double sampling to extract the video information from the pixels, analog control of 0dB to 34dB gain for varying illumination conditions, and black level clamping for an accurate black reference. The VSP2080 operates from 2.7V to 3.6V and is priced from \$2.25 @ 1Ku. Prod. now. Forward Concepts predicts that the worldwide digital camera market, which includes portable and PC-attached cameras, will grow to over 7 million units in '99 and 17 million units in 2001. Don Reynolds, strategic marketing engineer. [www.burr-brown.com](http://www.burr-brown.com)

**Cirrus** introduced an analog front-end interface chip (CS7620) that provides superior image quality and design flexibility for CCD digital still cameras. Designed in conjunction with **Polaroid** and **IBM**, the chip provides all of the functions necessary to bridge between the CCD and still-camera processor. IBM is the manufacturer of Polaroid's CCD designs. According to Semico Research the digital still camera market is expected to reach 6 million units in '99 growing to 26 million units in 2002. The CS7620 integrates all of the critical functions required to interface with a variety of CCDs: a correlated double sampler (CDS) for superior

image quality, a DRX enabled ADC for variable resolution images, a flexible on-chip timing generator, and two programmable DACs. Samples now, prod. in Q2. Douglas Holberg, director of Crystal Imaging and Video Products at Cirrus. Dr. Stuart Spitzer, director of Image Sensor Technology Division of Polaroid. [www.cirrus.com](http://www.cirrus.com)

**Conexant** announced a single-chip CMOS image sensor that provides high-resolution, XGA quality while lowering system costs and power requirements compared to CCDs for digital still cameras. The device provides superior visual quality with low noise performance, excellent color reproduction and 10-bit digital resolution. The sensor uses a small, 7-micron square pixel size that lets OEMs develop digital cameras with lower-cost half-inch system optics. The device operates at 3.3V and is claimed to be the only solution to integrate a 10-bit ADC and timing generator. A special windowing mode operates from 25 to 30 fps to provide an output for real-time LCD and digital zoom functions. Samples in Feb., prod. in March, \$30 @ 10Ku. Kevin Strong, senior VP and GM for the Personal Imaging Division. [www.conexant.com](http://www.conexant.com)

**Cypress** is sampling its entire family of Ultra37000 CPLDs. All devices will be in full production by quarter-end. The family is supported by Release 5.1 of Cypress's \$99 Warp2 VHDL-based design tools. The Ultra37000 family consists of 14 devices, ranging from 32 to 512 macrocells. It offers a fixed timing model that guarantees pin-to-pin propagation delays as fast as 5 ns for the 32-macrocell device, and 7.5 ns for the 256-macrocell device. The devices are available in 3.3-V and 5-V versions and offer In-System Reprogrammability, through a JTAG-compliant serial interface. Abundant routing resources enables pin-locking and "speed-locking" for all devices. Warp includes support for Jam, an open standard (sort of) that allows ATE and on-board microcontrollers to program the devices. Prices ranges from \$1.25 to \$49 in high-volume quantities. Christopher Norris, VP, PLD division. [www.cypress.com](http://www.cypress.com)

**DSP Group** unveiled its D16000 family of "System-On-A-Chip" DSPs. The new family provides customized solutions for advanced speech applications such as Digital Phones, Car Kits, Digital Answering Machines, Feature Phones, and Portable Digital Voice. The D16000 family of products is highlighted by a single IC comprised of an embedded DSP Core, analog CODECS, AFE circuitry, Host Controller func-

tionality and RAM/ROM memory. Due to the D16000 family's open architecture, OEMs can mix and match DSP functions from DSP Group's advanced, proprietary algorithms such as TrueSpeech Triple Rate Coder, Voice Recognition, True Full Duplex SpeakerPhone, Caller ID and CID on Call Waiting, FlexiSpeech playback, Least Cost Routing, Automatic Gain Control, and Call Progress and Tone Detection. Several major OEMs have already committed to new product lines based upon the D16000 family. Gideon Wertheizer, Corporate VP of Marketing, Jan Abelev, Director for Telephony Products. [www.dspg.com](http://www.dspg.com)

**DSP Group** unveiled the CT8016 DSP, featuring a low-cost, low-power G.729A+B Speech Processor. The device is targeted at Voice over Internet Protocol (VoIP) and Voice over Network (VoN) applications. In addition to the ITU-T standard G.729A+B (8 Kbps) — an optional Speech Coder for H.323 video and voice conferencing — the CT8016 also provides DSP Group's TrueSpeech Coder (8.5 Kbps) built into Windows 95/98 and standard G.711 PCM coders. Any Speech Coder can be used in full duplex mode simultaneously with acoustical echo cancellation for full duplex speakerphone applications, as well as telephony signal detection and generation. Victor Koretsky, Technical Marketing Director.

**GiGa** introduced the GD16361/GD16362, a 10Gbps transmitter and receiver chipset for SONET applications. The chipset takes up less than 60% of the area used by higher pin count PQFP packages and consume less than half the power of competing products. Coded-mark-inversion (CMI) enables system designs to meet and exceed SONET requirements at OC-3 rates in telecom-network applications such as cross connect and access boxes or in datacom applications including ISP Routers and ATMs. The CMI Interface is being widely deployed in Europe to reduce system costs by allowing the use of copper and eliminating the need for optics in short-distance applications. The chipset features a true Loss of Signal (LOS) detection as defined by the ITU-T G.775 standard and an on-chip equalizer working up to 300m RG-6/U cable. Available now. Bill Woodruff, VP of GiGa North America Marketing. [www.giga.dk](http://www.giga.dk)

**GlobeSpan** introduced the G2237 chipset for HDSL2 modem applications, which use Pulse Amplitude Modulation (PAM) techniques. The G2237 chipset is based on GlobeSpan's XDSL2 silicon platform, a fully programmable, high

density, low power design. The G2237 offers single wire pair multimode operation in either MSDSL or HDSL2 mode through firmware download. The chipset supports CAP, 2B1Q and PAM line codes for MSDSL, HDSL and HDSL2 applications. The G2237 chipset offers equipment suppliers a seamless migration path from MSDSL modems using 2B1Q or CAP line codes to an HDSL2 modem using PAM line code with OPTIS (Overlapped PAM Transmission with Interlocking Spectra) power density mask. It has been sampling since October '98. Angelo Stephano, VP of worldwide marketing. [www.globespan.net](http://www.globespan.net)

**Harris** announced 2 reference designs for building Class D audio amplifiers for the professional and home theater markets. They include a 125/220-watt full-bandwidth amplifier and a 250-watt subwoofer amplifier. Harris' Cool Audio Class D switching amplifier is more than 90% heat efficient. Alpine and Goldpeak are developing end products based on the technology. The ref. designs feature THD < 0.1% at 1kHz and 110W into 8 ohms, SNR > 110dB relative to full power, DC to 80 kHz small signal bandwidth and 28kHz power bandwidth, no crossover distortion, and a slew rate of 8V/( $\mu$ s). Patrick Begley, senior manager of audio products. [www.semi.harris.com](http://www.semi.harris.com)

**Hi/fn** (Nasdaq:HIFN) introduced a public key processing IC designed to speed up calculations used in public key cryptography for VPN and electronic commerce applications. The Hi/fn 6500 Public Key Processor contains a true random number generator and performs modular arithmetic more efficiently than any general purpose processor, completing 50,000 public key or 200 private key 1024-bit RSA computations per second. These functions are made available through a high-level cryptographic API. The 6500 is compatible with the most widely used key exchange and digital signature algorithms, such as RSA, Diffie-Hellman and DSA (Digital Signature Algorithm). Samples now. \$44.70 - \$64.70 @ 10Ku. Bob Monsour, VP of marketing. Tel: 408/399-3500, Fax: 408/399-3501, [www.hifn.com](http://www.hifn.com)

**IDT** announced a 20% price reduction for the TQFP-packaged RC3041 RISC controller, making it the industry's first 32-bit RISC processor priced in volume (100Ku) at less than \$5 (according to IDT). The RC3041 is currently used in EchoStar's DISH Network satellite digital receiver, Bay Networks' cable modems and Hughes' Direct PC. Phil Bourekas, director of

marketing and applications for the microprocessor division. [www.idt.com](http://www.idt.com)

**Intel** announced the Pentium III processor brand name for its next generation microprocessor code-named Katmai. Scheduled to be introduced later in Q1, the Pentium III processor offers enhanced multimedia realism. Katmai, a 32-bit processor, includes Streaming SIMD Extensions, a set of 70 new instructions designed to enhance 3D, imaging, and video applications. The Pentium III processor will use the slot 1 and slot 2 connector. In Q1 the Pentium III will be offered in 450- and 500-MHz slot 1 versions with a 512K L2 cache and a 100-MHz bus. Intel also disclosed the Intel Pentium III Xeon processor brand name targeted for the server and workstation market segments. Jami Dover, VP, Intel Sales and Marketing Group, and director, Worldwide Marketing Operations.

**Lexra** announced its next generation LX4180, a MIPS-R3000 class RISC processor core, architecturally compatible with the LX4080. It employs a 5-stage pipeline and executes all MIPS I instructions except for unaligned loads and stores. The core operates at 155 MHz, occupies 2.75 mm<sup>2</sup> and consumes 175 mW in a 0.25 $\mu$  process. The die size with 8KB of instruction cache and 8KB of data cache will be less than 10 mm-squared. In standby mode, the power consumption of the LX4180 is <50uW.

The LX4180 has several enhancements including: MIPS16 Instruction Compression, where most commonly used 32 bit instructions can be expressed in 16 bits, reducing program size by up to 40%. EJTAG Debug Support - When the microprocessor is deeply embedded inside of an ASIC, a common interface methodology, such as EJTAG is necessary. The LX4180 is one of the first RISC cores to implement 100% of the EJTAG 1.5.2 specification. The optional MAC engine for DSP applications can complete one MAC instruction every cycle without stalling the CPU pipeline.

The LX4180 also incorporates system friendly features including strict use of single edge clocking, flexible memory architectures and cache sizes, instruction extension capability, and, a flexible, PCI-like system bus. Lexra is focused on providing the design tools and methodology, system level interfaces, and silicon process portability that will enable easy integration of its processors into customer applications and claims that this is one of its major competitive advantages. The LX4180 will be available as a RTL core in Q1 and as a foundry optimized

SmoothCore beginning on Q2. A one project design license starts at \$325K. Charlie Cheng, president and CEO, Patrick Hays, VP and CTO. [www.lexra.com](http://www.lexra.com)

**Lucent** introduced the Everest 900MHz digital cordless chipset, which it claims will enable cordless phone manufacturers to deliver products with world class clarity and range at up to half today's typical costs. The programmable chipset consists of two B900 DSPs, two CSP1009 Communications Signal Processors (four-channel codecs), and two W9009 RF transceivers designed for the 900MHz ISM band. The B900 is a new 3.3V version of Lucent's DSP1609 (100MIPS DSPs), with additional memory. The chipset enables 6 hours of talk time and 7 days of standby time. Thomson Consumer Electronics and BellSouth will introduce phones using this chipset. The 900MHz digital cordless phone market is expected to grow at an estimated 57% annual rate through the year 2002, according to Forward Concepts. The market is expected to expand from an estimated 4.4 million units in '98 to 26.5 million units by the year 2002. The chipset is \$14.95 @ 100Ku. Samples now, prod. in Q1. Steve Kaufman, GM of consumer ICs.

**Mediamatics**, a National company, announced Pantera-DVD, a fully integrated DVD-On-A-Chip solution for consumer DVD players. Pantera-DVD integrates all the back-end functions of a typical DVD player, including host processing. Mediamatics also introduced a manufacturing kit with complete system software. Pantera-DVD is compatible with all six DVD regions and both the PAL and NTSC viewing standards. Pantera-DVD is fully compatible with all DVD specifications, CDDA, Video CD and China's emerging SuperVCD format, and supports a variety of audio standards including Dolby Digital AC3 and DTS. Pantera-DVD integrates a 32-bit RISC processor, Audio RISC-DSP, MPEG hardware, 10-bit Video DACs, graphics and NTSC/PAL encoder. Mediamatics has been working closely with several leading consumer electronics companies in Japan, Southeast Asia, South America and Europe which will announce Pantera-DVD-based players this quarter. Pier Del Frate, VP of marketing at Mediamatics. [www.mediamatics.com](http://www.mediamatics.com)

**Micrel-Synergy** introduced the SY87701V and the SY87700V, protocol-independent clock recovery ICs featuring output frequency ranges of 32Mbps to 1.25Gbps and 32Mbps to 175Mbps respectively. Both devices may be

## New Products

(Continued from page 17)

programmed to operate in a wide range of Bellcore-compliant frequency bands and operate at 3.3V or 5V. The low-jitter, devices can be programmed "on-the-fly" for any required frequency. Typical applications include the ports and backplanes of SONET, ATM, Gigabit Ethernet, and Fiber Channel equipment, fiber optic modules, and high-speed servers. Dona Flamme, dir. of marketing. [www.micrel.com](http://www.micrel.com)

**Photobit** announced 2 new products in its line of videoconferencing chips. The new sensors, the PB-100 and PB-300, are CIF-size (352 x 288) and VGA-format (640 x 480), respectively. Both employ Photobit's patented "active-pixel" technology as well as the company's proprietary TrueBit Noise Cancellation and TrueColor features. The sensors output color or monochrome full-frame 8-bit digital video at 30 fps. They feature electronic pan, tilt, and zoom, auto-exposure, and full programmability via a serial interface. The pixel array, the timing and control logic, and the ADCs are all on-chip. [www.photobit.com](http://www.photobit.com)

**PMC-Sierra** announced a Layer 3 upgrade for the EXACT Gigabit Ethernet and Fast Ethernet switching chipset. The EXACT AfterBurner upgrade allows users of PMC's EXACT chipset to support IPV4 forwarding for applications such as VLAN routing, IP Packet-Over-SONET (POS) switching or edge routing. AfterBurner provides the EXACT chipset with IPV4 Layer 3 routing capability, identification of higher layer protocols (such as OSPF, RIP, BGP, ICMP) and a Layer 3 Control and Management Interface to simplify the attachment of external CPU management resources. It supports up to 131,072 routes using a longest prefix matching algorithm, and provides a 512 entry ARP cache. The EXACT AfterBurner upgrade is available at no additional cost for systems using the EXACT chipset, consisting of the PM3370 octal 10/100 Ethernet port controller, the PM3380 Gigabit Ethernet port controller and the PM3390 and PM3391 EXACT bus switch matrix devices. Vernon Little, director of marketing for Ethernet Products. [www.pmc-sierra.com](http://www.pmc-sierra.com)

**Siemens** introduced the MUNICH 128X (PEB20324H), a 4-port, 128-channel version of its MUNICH 32 protocol controller IC. The MUNICH 128X is a 128-channel WAN Protocol Controller that provides 4 independent 24/32-channel HDLC Controllers, each with a ded-

icated 64-channel DMA Controller and a Serial PCM Interface Controller. The device can support up to 128 full-duplex serial PCM channels. The chip performs Layer 2 HDLC formatting/deframing at data rates from 8 kbps to 2.048 Mbps or V.110/X30 protocols up to data rates of 38.4 kbps. The MUNICH 128X is targeted at telecom and datacom applications, including routers, switches, access concentrators, and access equipment. Samples now, prod. later this quarter, \$62.35 @ 10Ku. Klaus Luecke, dir. of product development for Data Access.

**SMSC** introduced the LAN83C183, a 3.3V, 10/100 Mbps Fast Ethernet PHY. The LAN83C183 comes as a result of SMSC's relationship with **SEEQ** and is pin-compatible with SEEQ's TQ80223. Samples now. Robert Hollingsworth, VP of Marketing, Andy Lambrecht, Dir. of Strategic mktg. for LAN products. [www.smcs.com](http://www.smcs.com)

**Solidum** has launched its packet classification technology for multi-gigabit networks. Solidum has a packet classification language, compiler and interface card that enable developers to build devices that support classes and QoS. Solidum's technology facilitates a new generation of chipsets, NICs and networking equipment that can support more complex mixes of traffic and quality standards such as Differentiated Services (DiffServ). PAX is claimed to perform table lookups, access control, packet filtering and more at lower costs than alternative methods. PAX is based on a programmable state machine approach, is scalable and technology efficient. Solidum claims that PAX strikes the most cost-efficient balance between hardware and software for Packet processing. Solidum will initially target three groups: Developers of ICs and NICs, manufacturers of microprocessors, and manufacturers of networking equipment. Evaluation copies of packet classification technology based on the PAX language are available now. Pricing for the evaluation package begins at \$10K, to be applied towards the purchase of the development environment for \$49K. Solidum was founded in 1996 with private funding. Misha Nossik, VP, Business Development, Felix Welfeld, co-founder and CTO. [www.solidum.com](http://www.solidum.com)

**UMC Group** announced that it is the first foundry to offer the Direct Rambus ASIC Cell (RAC). Rambus has successfully fabricated and characterized the RAC in the form of test chips on UMC's 0.25u process. The Direct RAC delivers 1.6 gigabytes per sec over a 72-pin interface. The Rambus Direct RAC is part of UMC's

Gold IP program, meaning it is already being used by UMC customers. Customers that are seeking the Direct RAC must license it from Rambus. UMC also announced that in 1999 it will have production-ready 0.18u and copper-interconnect technology. Jim Ballingall, VP of worldwide marketing for UMC Group (USA). Tel: 408/733-8881, fax 408/733-8090, [www.umc.com.tw](http://www.umc.com.tw). Dave Mooring, VP and GM for Rambus' PC Division. [www.rambus.com](http://www.rambus.com)

**VLSI** introduces the VSC11 0.15u drawn gate length process. VSC11 features copper-based interconnect, embedded FLASH memory, digital, analog and RF mixed-signal capabilities and options to simultaneously optimize an IC for high-performance and minimal power consumption. VSC11 is a 0.15u drawn (0.12u effective) gate length process, with a fully contacted metal 1/2,3 pitch of 0.46/0.52-micron. The process uses up to five layers of metal for signal routing with a sixth layer supporting signal re-distribution for Flip Chip packaging. At an 80% silicon utilization, this yields 7.2-million logic gates per square centimeter of silicon area in 5-layer metal designs, double that of the 0.2u VLSI VSC10 process now entering full production.

VSC11 uses a low k dielectric material between metal lines on the same layer. VSC11 also offers the option of copper interconnect on the upper two layers of metal. VLSI studies have demonstrated that at 0.15u geometries, copper interconnect offers performance enhancements for relatively long routings for block-to-block connections, and power and clock distribution grids. At lower layers with shorter connection runs, aluminum interconnect retains competitive performance and remains less expensive to manufacture. VLSI will migrate to an all-copper interconnect strategy for process generations that follow VSC11.

VSC11 operates internally at 1.5V, with I/Os optimized for driving 3.3V with tolerance for 5V signals. VSC11 can also support a 1V core, for ultra low power applications. Dual-gate oxide technology enables 3.3V drive with 5V tolerant I/Os and is also used to enable analog circuits used on mixed-signal chips (majority of VLSI chips) to operate at 3.3V for improved dynamic range. VSC11 supports a cut-off frequency (fT) of greater than 65-GHz. Evaluation Libraries in Q1, production libraries in Q3. Prototypes in and production in Q4. Alfred Stein, chairman and CEO, Rajeeva Lahri, senior VP for corporate R&D. [www.vlsi.com](http://www.vlsi.com)

**Xilinx** announced the new XC9500XV family of 2.5V CPLDs. Manufactured on the latest generation FastFLASH process, the new XC9500XV CPLDs provide the same advanced architectural features and densities as the popular 3.3V XC9500XL family introduced last year, with device offerings of 36, 72, 144 and 288 macrocells. Evert Wolsheimer, VP/GM of the CPLD Business Unit. [www.xilinx.com](http://www.xilinx.com) ■

## Design Wins

**Harris** announced that its RF ICs will be incorporated into **ShareWave** wireless technologies aimed at the home networking market. The ICs will be utilized in ShareWave's Cresta Digital Radio, a key component of the ShareWave Digital Wireless technology portfolio. ShareWave envisions a central server (a PC, residential gateway or set-top box) serving as the Multimedia Furnace that wirelessly connects a variety of digital devices throughout the home. The chips are being used in ShareWave PC-to-PC and PC-to-TV product designs that allow multimedia data – including full-motion video and CD-quality audio – to be moved wirelessly at high speeds. The Harris chips allow 4Mbps data rates using direct sequence spread spectrum (DSSS). ShareWave and Harris are also exploring ways to integrate Harris' 11 Mbps chips into ShareWave's next generation product technologies. Ron Van Dell, VP/GM of Harris' Communications Products Business, Jim Schraith, ShareWave president and CEO. [www.sharewave.com](http://www.sharewave.com), [www.semi.harris.com](http://www.semi.harris.com)

**Sensory** shipped their one-millionth speech recognition chip in 1998. Since 1995, Sensory claims to have usurped 85% of the dedicated speech recognition chip business with applications in telephones, toys, clocks, light switches, electronic learning aids, automotive add-ons, security devices, PC peripherals, home automation and personal electronics. Sensory uses a proprietary neural network technology, which enables accuracy rates as high as 99% even in the presence of moderate background noise. Their custom IC designs incorporate all the speech recognition needs including, memory, processing, power, filtering amplification, digital and analog conversion, plus timing functions and a variety of I/O capabilities. Sensory's software solution can run on any DSP, with far less MIPS and memory requirements than comparable quality approaches.

Sensory design wins include Uniden's Voice-Dial Cordless Phones, Sony's Voice Controlled

Music System, Sega's Voice Lock-On Gun, VOS Systems' INTELAVoice voice-operated light switch, Sharper Image's Handheld Voice Dialer, Playmate's Voice Laser Gun and Radica's Girl Tech product line. Mark Frankel, VP of Sales. [www.sensoryinc.com](http://www.sensoryinc.com)

**Sierra Research and Technology** signed an agreement in which **Filanet** will license the Sierra Managed 10/100 Mb/s Stand-Alone Ethernet MAC. The agreement will allow Filanet to quickly produce, market and sell ASSP's based on Fast Ethernet technology. The Sierra 10/100 Ethernet MAC has been proven in more than a dozen semiconductor processes, and is shipping in PCI-based NIC applications, bridges, hubs, routers and other networking/data communication applications. The 10/100 MAC core has been licensed to numerous semiconductor manufacturers worldwide. Dr. Ken Friedenbach, Director of Engineering at Sierra. [www.srti.com](http://www.srti.com)

Filanet (Mountain View, CA) is developing IEEE-1394 and USB connectivity solutions for networking environments. Investment partners include Weiss, Peck and Greer, Menlo Ventures, Stanford University, and individual investors. Avner Ben-Dor, founder and CEO, was previously VP of Engineering at Kalpana. Rene Troncoso, Dir. of Product mktg., [renet@filanet.com](mailto:renet@filanet.com). Tel: 650/968-9711, [www.filanet.com](http://www.filanet.com)

**Sigma Designs and Boca Research** announced that the new BocaVision ST2001 PC Internet/information appliance, or set-top box, incorporates Sigma Designs' EM 8220 DVD/MPEG-2 decoder chip for DVD and MPEG playback. The ST2001 provides Web browsing, email sending/receiving, PC functions, and DVD audio and video CD playback. The BocaVision ST 2001 features Network Computer's feature-rich, open Internet standards-based TV Navigator. Beta testing in Q1, volume shipments in Q2.

Using NCI's TV Navigator software along with the Oracle Video Server and Sigma Designs' REALmagic MPEG decoding technology, the ST2001 achieves full motion 30 fps streaming video with an easy-to-use Web-based interface, giving service providers the ability to deliver on-demand movie channels and new interactive video services. IDC estimates that the information appliance market will reach a penetration level of over 41 million units by the year 2002. William Wong, Sigma Designs' VP of marketing. Tom Elowson, director of marketing for Boca Research. [www.sigmadesigns.com](http://www.sigmadesigns.com)

**Virata's Helium** Integrated Software on Silicon (ISOS) has been selected by **OpenCon** Systems, for OpenCon's next generation of ADSL products for Local Exchange Carriers and ISPs. OCS will use Virata's Helium ISOS solution for its new family of line card and gateway Access Technology Products. Helium is a low-cost, phy-neutral chip that provides high-speed access capability for multiple-user endpoint devices such as modems, gateway devices, and line cards for channel banks and DSLAMs. OpenCon Systems, Piscataway, New Jersey, was founded in 1991 and is a turnkey provider of Transmission and Access, Network Management and Communication Software Solutions to the communications marketplace. Oleg Logvinov, Dir., Product Development for OCS. Charles Li, Senior Director, Access Technology Products for OCS. Martin Jackson, Virata's CTO. [www.opencon.com](http://www.opencon.com), [www.virata.com](http://www.virata.com) ■

### Philadelphia SOX Index



### Intel



### Texas Instruments



### Micron





# Company Financials

Company	Symbol	Current Qtr.				Last Qtr		Yr ago qtr		Sales Growth	Net Growth	Qtr	Ending
		Sales	Net	Margin	GM	Sales	Net	Sales	Net				
Seeq	SEEQ	6	-1.3	-23%	25%	7	-6.9	8	1.1	-26%	-218%	1Q99	31-Dec
SMSC	SMSC	45	0.8	2%	32%	41	0.6	43	-2.0	6%	-140%	3Q99	30-Nov
SST	SSTI	18	-6.7	-37%	-3%	18	-7.3	20	-3.8	-10%	76%	4Q98	31-Dec
ST Micro	STM	1,133	122.0	11%	38%	1,039	101.6	1,104	126.0	3%	-3%	4Q98	31-Dec
Stanford Telcom	STII	37	-0.5	-1%	19%	41	0.3	41	1.6	-9%	-131%	3Q99	31-Dec
Supertex	SUPX	12	2.2	18%	45%	13	2.2	14	2.4	-14%	-8%	3Q99	31-Dec
T.I.	TXN	1,993	189.0	9%	44%	2,113	164.0	2,428	-285.0	-18%	-166%	4Q98	31-Dec
Telcom	TLCM	12	-0.3	-2%	31%	13	-6.1	15	1.9	-19%	-116%	4Q98	31-Dec
Tower	TSEMF	17	-4.2	-25%	-13%	15	-4.9	31	4.3	-46%	-198%	4Q98	31-Dec
TranSwitch	TXCC	14	2.5	18%	64%	12	1.9	8	0.4	65%	525%	4Q98	31-Dec
Trident	TRID	21	-1.8	-9%	39%	24	-2.7	27	-1.9	-23%	-5%	2Q99	31-Dec
Unitrode	UTR	40	-2.9	-7%	47%	30	3.0	59	10.5	-32%	N/A	3Q99	31-Oct
Vitesse	VTSS	60	15.4	26%	62%	54	16.5	35	10.4	73%	48%	1Q99	31-Dec
VLSI	VLSI	138	14.8	11%	38%	131	-3.6	193	22.0	-28%	-33%	4Q98	25-Dec
Xicor	XICO	27	-10.0	-37%	14%	25	-8.0	31	-7.5	-14%	33%	4Q98	31-Dec
Xilinx	XLNX	167	33.9	20%	61%	156	27.8	149	31.6	13%	7%	3Q99	2-Jan
Zilog	ZLG	54	-17.1	-32%	27%	53	-21.7	59	0.4	-8%	-4863%	4Q98	31-Dec
Zoran	ZRAN	14	0.9	6%	55%	12	0.4	14	1.7	1%	-47%	4Q98	31-Dec

**Notes:** Sales growth = current qtr. sales / yr-ago qtr sales.  
All sales figures are rounded to the nearest million  
Net growth = current qtr. net inc. / yr-ago qtr. net inv.  
GM = current qtr. gross margin.

1) Motorola and Linfinity Net represent operating income

# Company Rankings

	<u>NET MARGIN</u>		<u>GROSS MARGIN</u>		<u>SALES GROWTH</u>		<u>NET PROFIT (\$M)</u>	
<b>Top Ten</b>	Linear Tech.	38%	MIPS	99%	Broadcom	305%	Intel	2,064
	Maxim	32%	Rambus	80%	RF Micro Devices	212%	T.I.	189
	Galileo	31%	PMC-Sierra	78%	3Dfx	172%	ST Microelectronics	122
	MIPS	27%	Linear Tech.	72%	Mitel	140%	ATI	50
	Intel	27%	MMC Networks	71%	ATI	95%	Maxim	47
	Vitesse	26%	Hi/fn	70%	MMC Networks	79%	Linear Tech.	46
	PMC-Sierra	25%	Maxim	68%	Vitesse	73%	Altera	43
	DSP Group	25%	AMCC	65%	TranSwitch	65%	Xilinx	34
	Altera	25%	QLogic	64%	Level One	55%	AMD	22
	QLogic	23%	Galileo	64%	QLogic	45%	Int'l Rectifier	20
<b>Bottom Ten</b>	<u>NET MARGIN</u>		<u>GROSS MARGIN</u>		<u>SALES GROWTH</u>		<u>NET PROFIT (\$M)</u>	
	Tower	-25%	Conexant	25%	Seeq	-26%	Aspec Tech.	-6
	Zilog	-32%	Stanford Telcom	19%	VLSI	-28%	SST	-7
	8x8	-32%	Alliance	19%	ISSI	-32%	Elantec	-8
	SST	-37%	ISSI	15%	Aspec Tech.	-33%	Oak	-10
	Xicor	-37%	Xicor	14%	Cirrus	-36%	Xicor	-10
	Oak	-44%	SST	-3%	Exar	-41%	Zilog	-17
	Cirrus	-60%	Cirrus	-12%	Tower	-46%	Conexant	-57
	Elantec	-75%	Tower	-13%	Alliance	-46%	S3	-70
	Aspec Tech.	-150%	S3	-40%	Oak	-56%	Cirrus	-93
S3	-169%	Aspec Tech.	-50%	S3	-59%	Mot. (semis)	-1,225	

# Startups In This Issue

- ✓ **C-Port** – *Communications Processor Platform*
- ✓ **Cognitive Designs** – *Cryptographic Chips*
- ✓ **Imsys** – *Triple ISA Microcontroller with Java*
- ✓ **IONAS** – *Optical Components and DFB Fiber Lasers*
- ✓ **ITRAN** – *Power Line Modem ICs*
- ✓ **Opticom** – *All-Organic Polymer Memory*
- ✓ **RC MODULE** – *NeuroMatrix Super-Scalar Processor*
- ✓ **Seagull Semi** – *System-on-Chip Products*
- ✓ **Sybarus** – *SONET ICs and Software*
- ✓ **TeraGen** – *Thread Processors*

**General:** *Semiconductor Times* is published monthly. Each issue contains profiles on startups and emerging semiconductor companies, industry news, financial and investment highlights. Subscribers receive names, addresses, telephone numbers and web sites of the featured companies.

**Subscription information:** Subscriptions in the USA, Canada and Mexico: \$497 for 12 months (12 issues). All other countries: \$545. Payments must be made by a check payable to *Semiconductor Times, Inc.* in U.S. funds drawn on a US bank, credit cards, or wire transfer. Call for site licenses and bulk rates.

**Payment Acknowledgement:** Invoices and credit card receipts are included with all orders. Contact us if you need a duplicate.

**Back Issues:** \$30 for 1, \$80 for 3, \$150 for 6, \$225 for 12 and \$15 for each additional issue.

**Publisher:** Cliff Hirsch

**Address:** 52 Pine St., Weston, MA 02493, USA  
**Tel:** 781/899-6613, **Fax:** 781/899-6357  
**Email:** info@semiconductortimes.com  
**Web:** http://www.semiconductortimes.com

**Schedule:** *Semiconductor Times* is mailed first-class the first week of each month.

**Missing Issues:** Please contact us for a replacement if your issue was lost in the mail.

**Change of address:** Notify *Semiconductor Times* at least two weeks before address changes. Provide the old and new addresses and the name of the subscriber who is moving.

**Reprints:** Contact us for details.

**ISSN** 1097-2927

**Copyright** © 1999, Pinestream Communications, Inc., all rights reserved. The title and words *Semiconductor Times* are claimed as trademarks. No part of this publication may be reproduced, copied, photocopied, scanned, stored in a retrieval system, or transmitted in any form or by any means (including internal distribution) without *Semiconductor Times'* prior written permission. Copying this publication is in violation of federal copyright law (17 USC 101 et seq.). Violators may be subject to criminal penalties as well as liability for substantial monetary damages, including statutory damages up to \$100,000 per infringement, costs and attorney's fees.

Take advantage of your subscription. Do you have a question? Are you searching for a company? Do you need an objective "sounding board" other than your co-workers and spouse? Contact us via phone, fax or email. We want to hear from you!

**Fee:** \$497 (USA, Canada, Mexico) or \$545 (All other countries). **Mail to:** *Semiconductor Times, Inc.*, 52 Pine Street, Weston, MA 02493, USA. **FAX** credit card orders to 781/899-6357. **Please type or print legibly.**

Name: \_\_\_\_\_ Title: \_\_\_\_\_

Company: \_\_\_\_\_

Address: \_\_\_\_\_

City, State/Province, Zip: \_\_\_\_\_ Country: \_\_\_\_\_

Tel: \_\_\_\_\_ Fax: \_\_\_\_\_ Email: \_\_\_\_\_

Check payable to: **Semiconductor Times, Inc.** (U.S. currency, drawn on a U.S. bank please.)

Visa  Mastercard  Amex Credit Card #: \_\_\_\_\_ Exp. Date: \_\_\_\_\_

Name as it appears on Card: \_\_\_\_\_

Signature: \_\_\_\_\_

Referred by: \_\_\_\_\_